PHILIPS TECHNICAL TRAINING

L05 ATSC TRAINING MANUAL

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NTSC SYSTEM

To better understand the ATSC system, a short discussion of the present day NTSC system would be helpful.

A committee set up by the FCC in 1939 approved the present NTSC (National Television System Committee) television system. Except for the addition of Color, Stereo, Closed Caption, and Text, the NTSC system has changed very little.

The NTSC system is based upon a scan rate of 30 frames per second with a four by three aspect ratio. The aspect ratio is the ratio of the picture width, which is four, and the picture height, which is three. This aspect ratio is based on 16mm film which was the most widely used form of visual entertainment at the time television was being developed.

The scan rate of 30 frames per second is achieved by the picture being scanned with 262.5 lines at a vertical rate of 59.94 times per second. (Figure 1) The picture is scanned with two fields using an interlace scan making 525 lines per frame. With the number of scan lines used, flicker would develop if interlace scanning were not used. The even field starts in the upper left hand corner. The Odd field starts its scan in the upper center portion of the picture. Because 40 horizontal lines are used for Closed Captioning, Teletext, and Color Correction, there are only 242.5 lines in each field that are actually visible.

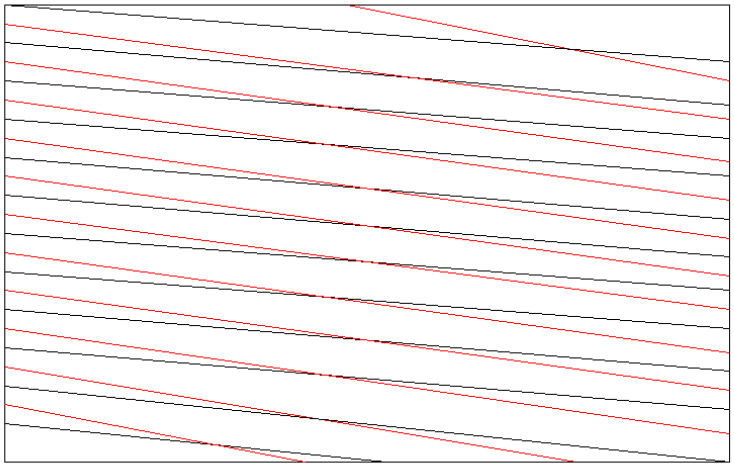


FIGURE 1 - INTERLACE SCANNING

ATSC SYSTEM

The Digital broadcast system, also know as ATSC (Advanced Television System Committee), delivers a high quality picture using complex video and audio compression.
The ATSC channels use the same UHF frequencies and 6 Mhz bandwidth as the NTSC channels.

There are two types of sets sold today, HD ready and Integrated. HD Ready sets do not have an ATSC tuner, but are capable of displaying a High Definition picture. These sets show an enhanced picture when used with a progressive scan DVD player. However, this is not High Definition. A set top box is required to received the Digital TV broadcast. The Integrated sets have the ATSC Digital tuner built in.

As required by the FCC, all stations are co-broadcasting the Digital channels. If the plan is followed, all NTSC transmission in the United States will end on December 31, 2006.

When viewing the new ATSC receivers, the first difference one would notice is the wider screen. The ATSC receiver has an aspect ratio of sixteen by nine. The screen width is 16 units and the screen height is 9 units. NTSC uses a 4 by 3 aspect ratio. The next noticeable difference would be a much sharper image. The picture definition of an ATSC receiver is measured in the same way as is in a computer monitor. The highest definition in the ATSC receiver is 1920 pixels in the horizontal direction by 1080 lines. The NTSC display measured in pixel resolution would be 313 by 243. The possible compression formats for the ATSC system are shown in Table 1 below. Although the ATSC tuning system is capable of receiving these formats, the AV inputs are more limited as will be discussed later. Notice that both progressive and interlace scanning are possible. Whichever format is being transmitted, the Philips L05 ATSC chassis will convert the aspect ratio to 1080 by 1920 pixels with a Picture Rate of 60I. That is 1080 interlace scanning with two fields, each having 540 visible lines. Some signals may broadcast a 4:3 aspect ratio picture with sidebars. The actual picture being transmitted has a 16:9 aspect ratio. However, the visible picture will have a 4:3 aspect ratio.

Vertical lines	Pixels	Aspect ratio	Picture rate
1080	1920	16:9	60I, 30P, 24P
720	1280	16:9	60P, 30P, 24P
480	704	16:9 and 4:3	60P, 60I, 30P, 24P
480	640	4:3	60P, 60I, 30P, 24P

TABLE 1 - PICTURE FORMATS

Only the 1080i and 720P formats are considered to be High Definition signals. All other formats are considered to be a Standard Definition format. The 480 x 640 and 480 x 720 formats are equivalent to the 480P or progressive scan outputs of DVD players. The NTSC signals are converted by this set to 1080i before being fed to the CRT. If a weak signal is present, artifacts may become more visible.

BANDWIDTH

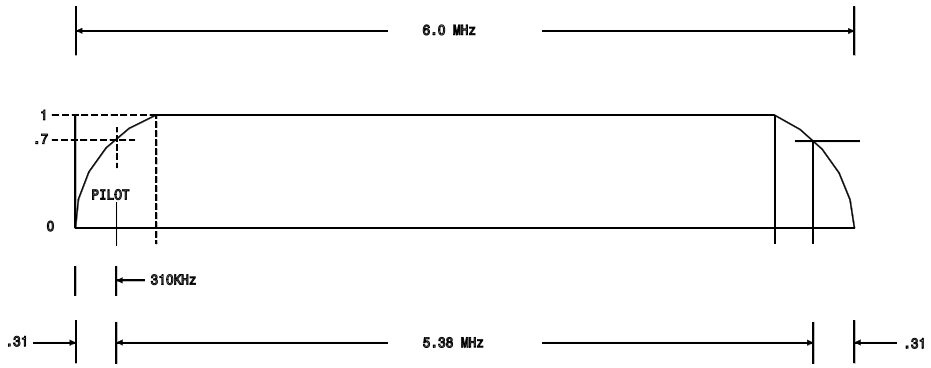


FIGURE 2 - ATSC FREQUENCY SPECTRUM

The ATSC signal uses the same six megahertz bandwidth as the NTSC signal. (Figure 2) To achieve the higher resolution of the ATV system, up to 19.28 Mbps (Mega bits per second) of data is delivered with the Terrestrial broadcast system. A higher data rate of 38.57 Mbps is possible when using cable or satellite. The higher data rate system also uses the same six megahertz bandwidth. A Pilot signal is added 310 kilohertz from the lower edge of the band to key the AFT circuit of the receiver. The Pilot signal power is 11.3 dB

below the data signal power. To reduce interference with NTSC channels, the ATSC signal is offset by +45.8KHz. After processing, the transmitted data signal has a bandwidth of 5.38 MHz.

ATSC BROADCAST ENCODING

As with NTSC signal processing, the ATSC signal starts out with analog Red, Green, and Blue drives from the signal source. (Figure 3) The signal source could be a Camera, Tape Deck, or one that is computer generated. The signal could be either the higher resolution HDTV or the lower resolution SDTV from a Composite NTSC signal. These signals are fed to a Matrix which produces a Y (luminance) signal, a Pr (red), and a Pb (blue) signal. These three signals are fed to their respective A/D (analog to digital) converters. If the RGB signals are of HDTV origin, the luminance-sampling rate for the A/D converters is 74.25 MHz. For signals from an SDTV source, the sampling rate is 13.5 MHz. These signals are then fed to an MPEG-2 compression system to reduce the amount of data necessary to broadcast the signal. In a similar manner, six channels of audio are fed to their respective A/D converters and then to the AC-3 audio compression system. The Video, Audio, Text, and Control data streams are combined into a single data stream by the Multiplexer.

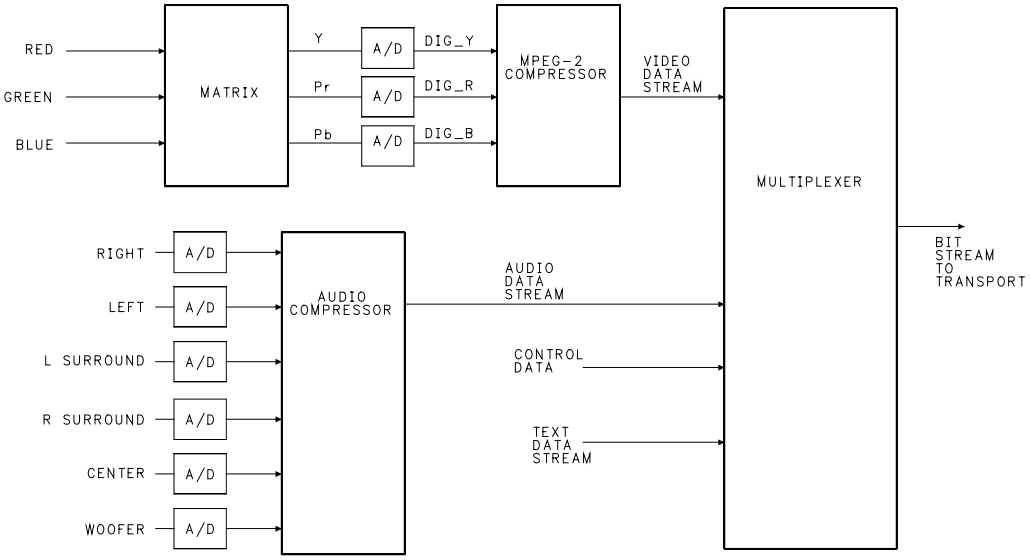


FIGURE 3 - ATSC ENCODING

ATSC COMPRESSION

The ATSC system uses the MPEG-2 compression format. It uses a 4:1:1 digital sampling system. (Figure 4) For every four Luminance samples, two Chroma samples are taken. These samples are placed in 8 x 8 arrays containing 64 samples. By using a complex mathematical function called a DCT (Discrete Cosine Transform), the amount of data needed to store an array is reduced. Four Luminance Arrays and two Chroma Arrays make up one Macro block. In the 1080 by 1920 display mode, there are 68 rows of Macro blocks and 120 blocks per row. In the SDTV mode which is 640 by 480, there are 30 rows with 40 blocks per row displaying 1200 Macro blocks.

The Macro blocks make up an "I" (Intra) frame or a complete frame of video. (Figure 5) If

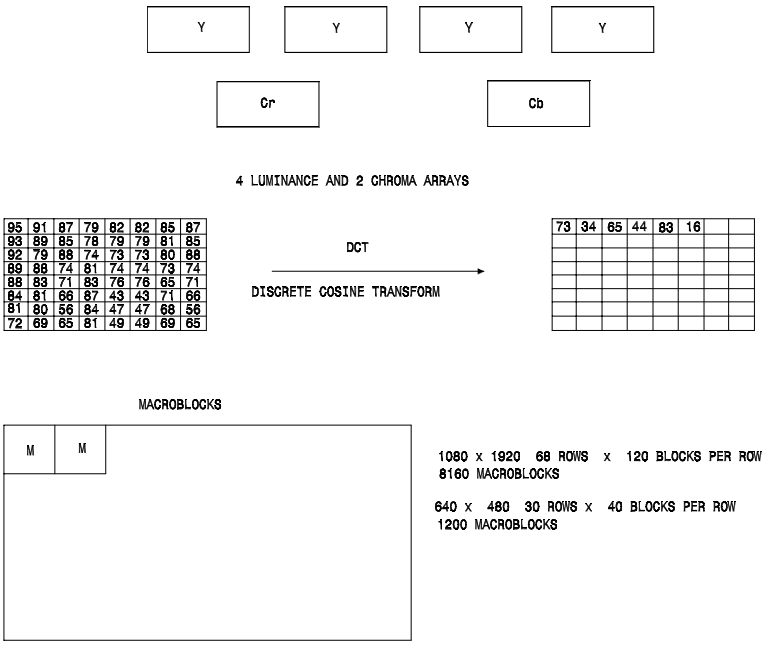


FIGURE 4 - COMPRESSION

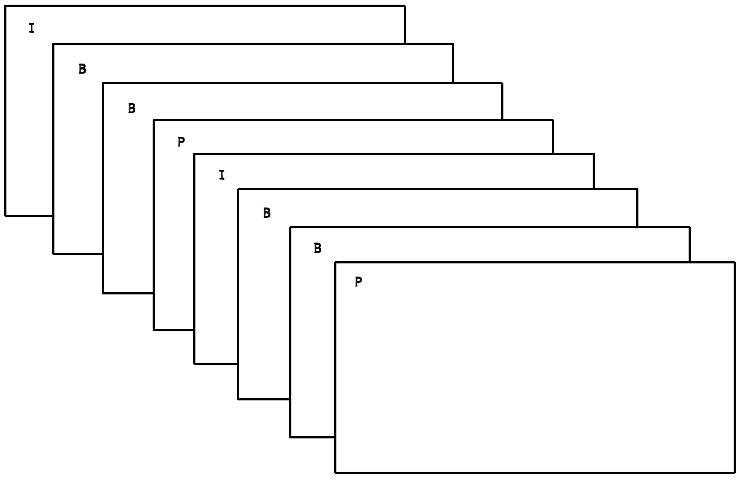


FIGURE 5 - FRAME ORDER

there is very little change in the video for the next three frames, the next two frames are skipped. Only changes in the "I" frame are placed in the "P" (Predictor) frame. The "B" frames or the skipped frames are reconstructed in the receiver.
The Video and Audio data streams along with the Control and Text Data are fed to the Multiplexer which produces data packets that are 187 bytes in length containing information from all four sources. All Picture, Audio, Control, and Text information are now in a single data bit stream.

TRANSPORT

To prevent data loss in transmission, there are four Forward Error Correction circuits. (Figure 6) The four are the Data Randomizer, Reed Solomon encoder, Data Interleaver, and Trellis Encoder. In the High Data rate system, there are only three Forward Error correction circuits. The Trellis Encoder is replaced by a map per in the High Data rate system. The output of the Forward Error correction circuits are fed to a Multiplexer as an eight level digital data stream in the Terrestrial system. In the High Data Rate system, this is a sixteen level digital data stream. The Multiplexer adds data segment and data field sync. This Sync is for data signal synchronization and has no relationship to the scan rate of the TV receiver. The Scan rate and Synchronization of the picture and audio are encoded in the video data stream. The Pilot is then added to the signal before it is sent to the Modulator and Up Converter. The Pilot is used to key the AFT circuit in the receiver.

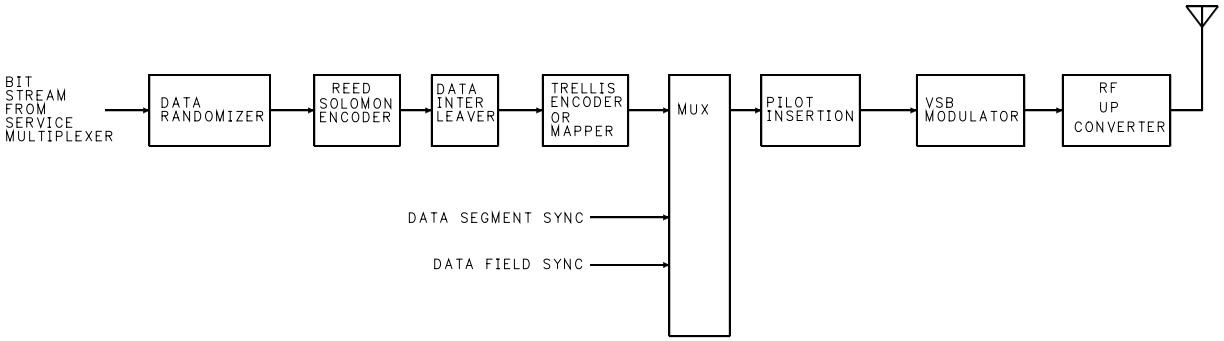


FIGURE 6 - TRANSPORT

DATA STRUCTURE

The Data Symbols are grouped into Data Frames, each containing two Data Fields. (Figure 7) Each Field contains 313 Data segments. Each Segment begins with 4 symbols to provide segment synchronization and 828 Symbols of Data. The 828 Symbols of the data segment contains the data of the 187 bytes of a transport packet and the Forward Error Correction overhead. In the Terrestrial broadcast system, the Symbols are an eight level signal, each carrying 3 bits of data. In the high data rate system, the symbols are a 16 level signal, each carrying 4 bits of data. Each Data field is separated by a sync segment. The Data Segment Sync is 4 symbols wide. (Figure 8) Three bits of data are mapped into 8 level VSB symbols. The voltage level of each symbols represents a 3 bit data code. Since the Trellis encoder changes each 8 bit word to a 12 bit word, 4 symbols are required to represent one byte of data. At the start of each Data Field, the Data Segment contains Field Data information and voltage reference levels to

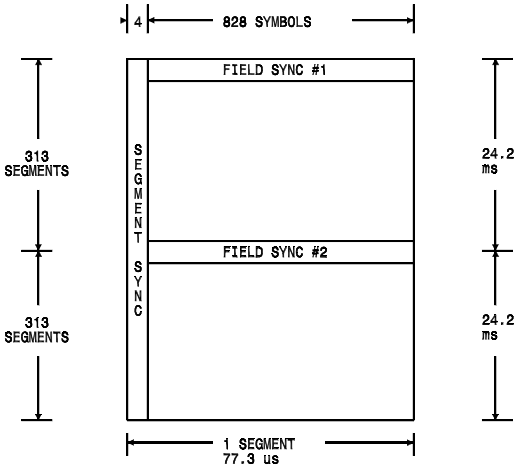


FIGURE 7 - DATA FIELDS

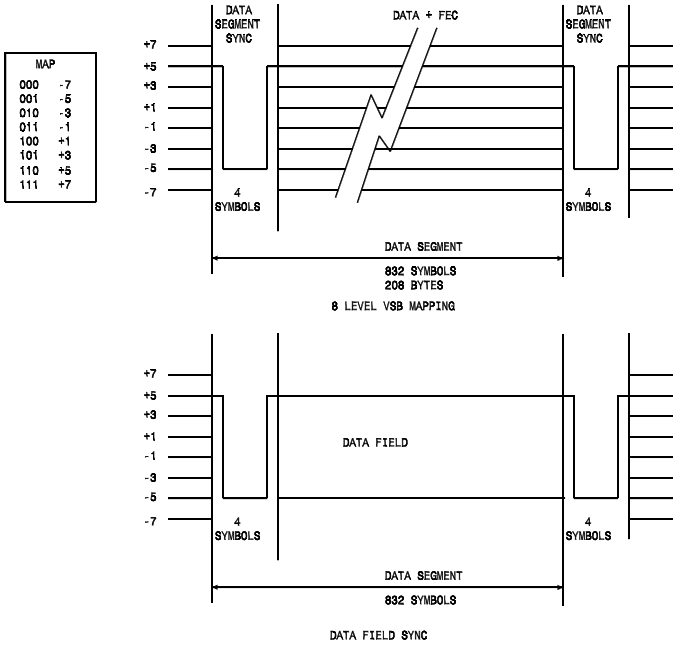


FIGURE 8 - 8VSB SEGMENT ENCODING

train the data recovery circuits in the receiver.

Since the picture and audio information is in a Digital form, there will not be a problem with Ghosting or Snow as with the present analog NTSC signal. Once sufficient signal is detected by the ATSC receiver to operate the set, a clear picture will appear on the screen.

RECEIVER INPUT

In the receiver, the ATSC signal is fed to the Tuner from an Antenna, Cable, or Satellite. (Figure 9) The Tuner receives the ATSC signal and down-converts it in much the same

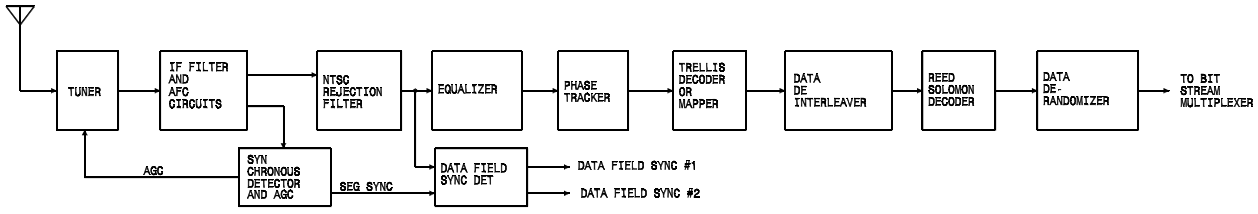


FIGURE 9 - ATSC TUNER

manner as in the NTSC tuner. The output of the Tuner, approximately 44 MHz, is fed to the IF filter and AFC circuit to separate the Pilot and Data signals. The Pilot is used to drive the Automatic Frequency Control circuit to adjust the frequency of the 2nd mixer in the Tuner. A precise frequency and phase lock is necessary to recover the Data from the signal.
The output of the IF circuit is fed to the Synchronous Detector and AGC circuit. It separates the Segment sync and provides AGC control for the Tuner. The level of the Segment sync keys the AGC circuit which feeds a DC control voltage back to the Tuner. The data signal from the IF circuit is also fed to an NTSC rejection filter. If the filter detects NTSC interference, the circuit is switched On. If no interference is detected, the filter is switched Off. The output of the NTSC rejection filter is fed to the Equalizer and the Data Field sync recovery circuit. The Data Field sync recovery circuit is also synchronized by the Segment sync from the Synchronous detector. The Data Field sync detector has as its output, Data Field sync one and Data Field sync two. This sync has no relationship to the scan rate of the TV display. It is used to provide sync for data recovery. The picture will be processed and appear on screen once the Data Field Sync is detected. The output of the NTSC rejection filter is also fed to the Equalizer. The Equalizer compensates for linear channel distortions, such as tilt and ghosts. The output of the Equalizer is then fed to the Phase Tracker and Trellis Decoder or Map per. The Trellis Decoder is used when the signal is an eight level terrestrial broadcast signal. The Trellis Decoder is switched Off and a map per is used if the signal is a higher rate sixteen level 38.8 Mbps data rate signal. These circuits change the eight or sixteen level signal back to an eight bit data signal. The signal is then fed to the Forward Error correction circuits which are the Data De-Interleaver, Reed Solomon Decoder, and Data De-Randomizer. This is the reverse order that was used by the Forward Error correction circuits in the transmitter.

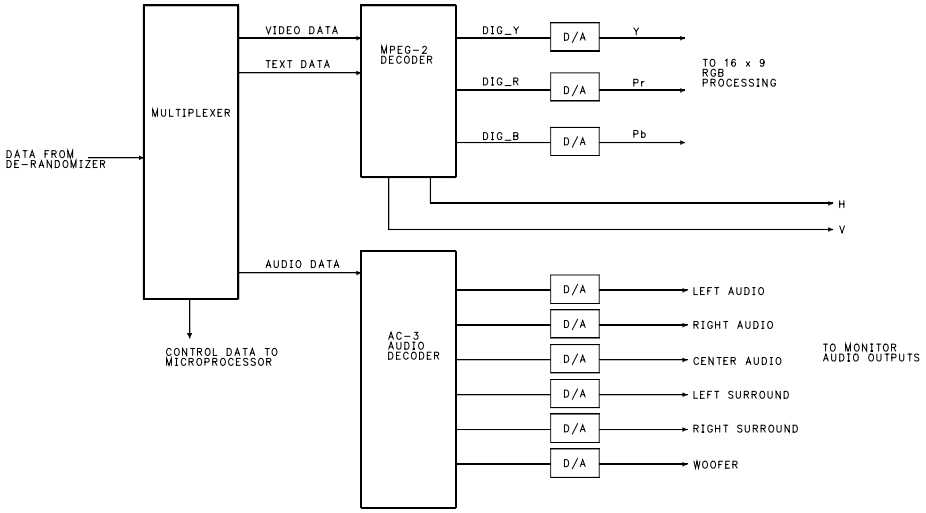


FIGURE 10 - DECODING

The output of the Data De-randomizer is fed to a Multiplexer, which separates the Video, Text, Audio, and Control data bit streams. (Figure 10) The MPEG-2 decoder decompresses the Video data bit stream to produce a digital Y, R, and B signals. These signals are fed to their respective Digital to Analog (D/A) decoders. The signal is now analog at this point. The analog Y, Pr, and Pb signals are then fed to the monitor section. Horizontal and Vertical sync from the decoder are also fed to the monitor to operate the sweep circuits. The Audio bit stream is fed to the AC-3 decoder which produces six digital audio output signals. These are fed to their respective digital to analog decoders. Six analog audio signals are then output to the monitor.

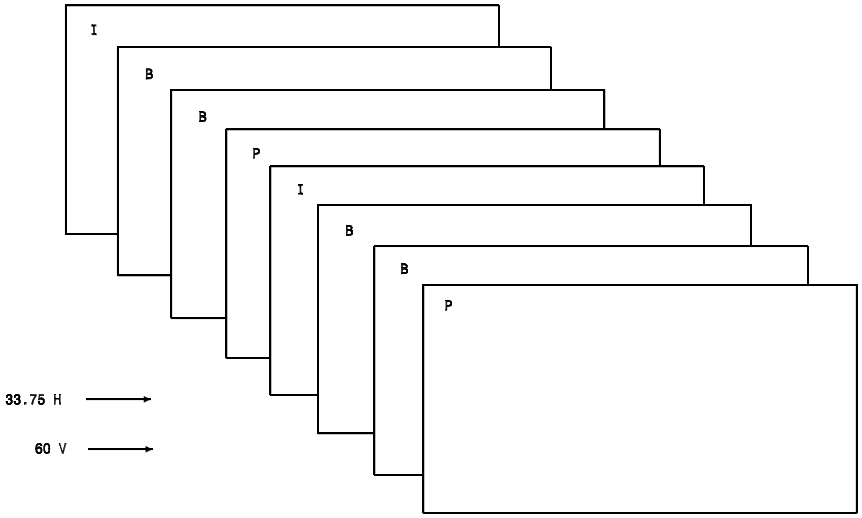


FIGURE 11 - RECEIVE FRAME ORDER

The decoder decompresses the "I" frames of video and stores it in memory. (Figure 11) The decoder then processes the "P" frame and "I" frame to produce a complete frame of video for the "P" frame. The "I" and "P" frames are interpolated to recreate the two "B" frames of video. Once four frames are processed, they are read by the sync generator to produce the "Y", "Pr", and "Pb" outputs to the monitor. The frames are stored in the 1080 by 1920 format by the DPTV120 decoder. The DPTV 110 monitor uses a 1080 interlaced display. The odd lines are read for the first field and the even lines are read for the second field. Each field displays 540 lines.

The Control data bit stream from the Multiplexer is fed to the Microprocessor. The Control data contains information about the transmitted signal. For example, the number of Bit streams, the Compression format used, Channel guide information, and the Closed Caption

information. When the signal is transmitted in the lower bit rate SDTV mode, four or more video and associated audio bit streams can be transmitted. This allows up to four sub-channels in each channel.
L05 ATSC CHASSIS

ATSC Cable Transmission

The previous material shows the 8VSB terrestrial broadcast system. Since cable TV is a closed system, a faster data transfer method can be used. The 8VSB system can transmit a maximum of 19.2 megabits of data per second.

Cable uses either 64QAM or 256QAM to distribute digital TV data. This system uses a combination of amplitude and phase modulation to transmit the signal. Compression methods and error correction are the same as with the 8VSB system.

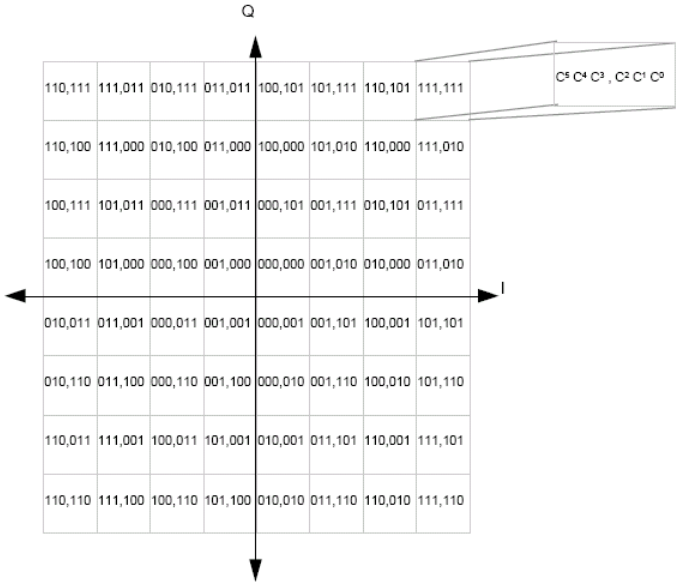


FIGURE 12 - 64QAM

The 64QAM system is shown in Figure 12. The 64QAM system is capable of a data transfer rate of 26.97 megabits per second.

Figure 13 shows the 256QAM mapping. The 256QAM system is capable of transmitting 38.4 megabits per second.

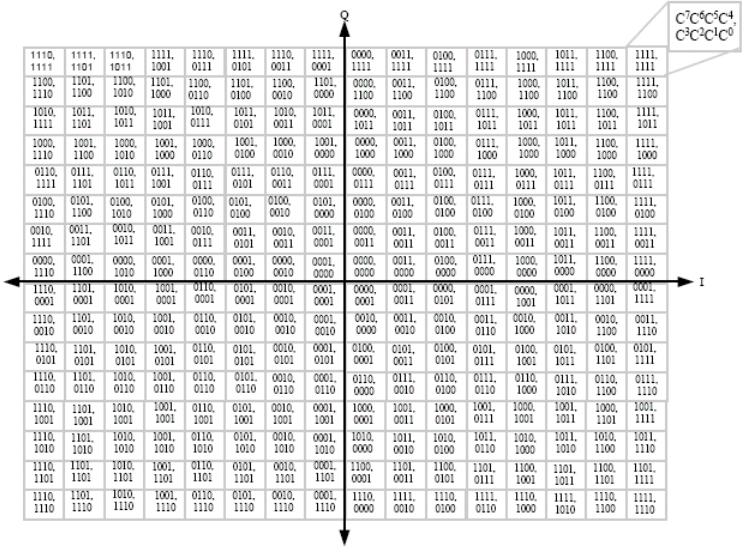


FIGURE 13 - 256QAM

Introduction

The L05 ATSC chassis is designed for the model year 2005. This set has a fully integrated ATSC as well as a NTSC tuning system. This set will come in a 26 and 30 inch screen sizes in a 16x9 format. There will be a 32 inch version using a 4x3 ratio screen.

The set consist of a Main panel, CRT board, Side I/O panel, ATSC module, and Deflection controller panel. The panels consists primarily of conventional components with some surface mounted devices.

The functions for the 1fH video processing is performed in one IC (TDA1200xx, IC7200), the Hercules chip. This IC is located on the solder side of the Main panel. NTSC tuning and switching for AV1, AV2, and CVI inputs are performed on the Main panel. The CVI input located on the Main panel are for 1fH (480i) signals only.

The ATSC Tuner and 1fH to 2Fh conversion is performed on the ATSC module. Component inputs for the CVI HD and HDMI are located on the ATSC module. This input can accept 480i, 480p, 1080i, or 720p signals. The ATSC module converts whatever signal is applied to a 1080i format. The ATSC tuning system can tune all channels in the VHF, UHF, and Cable bands.

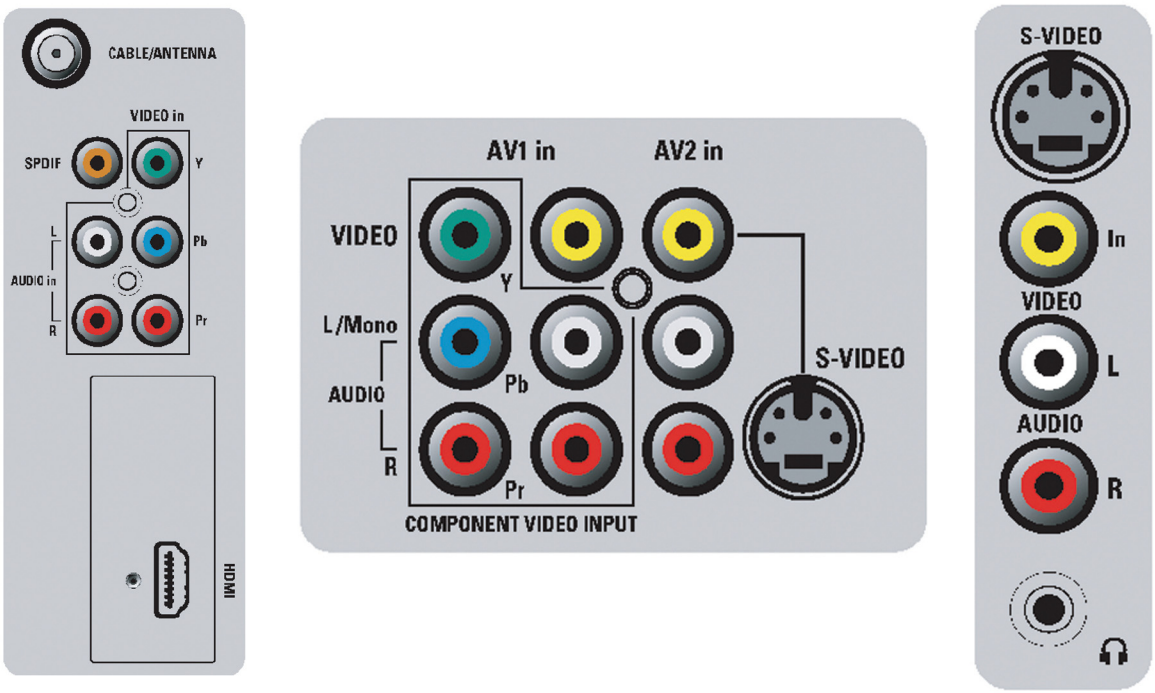
The Microprocessor communicates with the memory IC located on the Main panel, Keyboard, Remote Receiver, NTSC Tuner, Deflection Controller panel, and ATSC module. The Memory IC retains the settings for favorite stations, customer-preferred setting, and circuit settings. The circuit settings can be accessed by the service technician via the Service Alignment Mode.

On-screen graphics and Closed Caption decoding are performed in IC 7200 for NTSC. IC 7200 is located on the Main signal panel. On-screen graphics and Closed Caption for the ATSC channels are performed in the ATSC module.

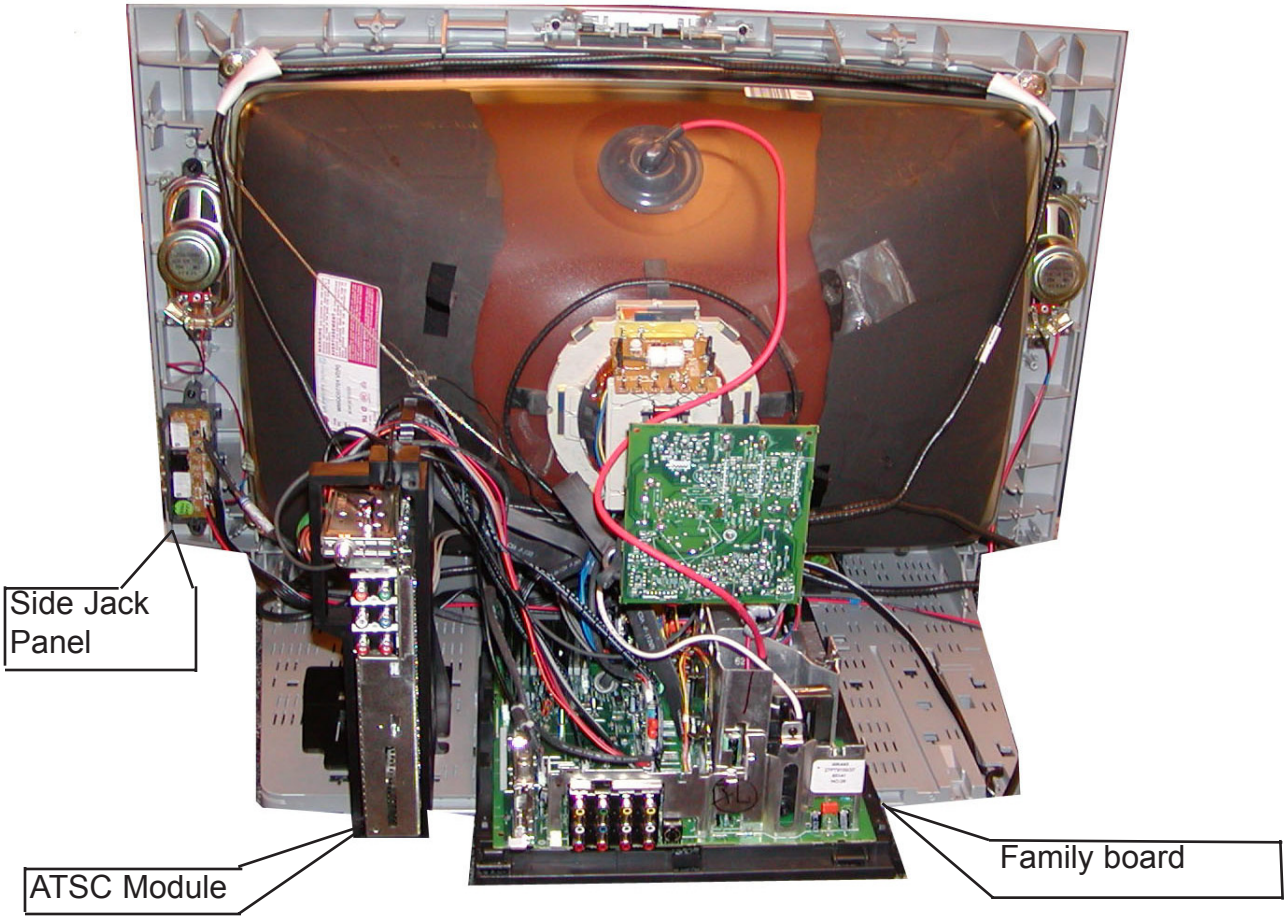
Customer Operation

There are two different menu structures in the L05 ATSC, one for the Analog and one for the Digital mode. Press the A/D button on the Remote control to toggle between the two modes. There is no selection in menu to switch between Digital and Analog. It can only be performed with the Remote.

The Digital channels may have one or more subchannels if the station is transmitting in the SDTV mode. The customer must press the A/D button to place the TV in the Digital mode. Then press the channel number followed by a period and the sub channel number. If the station is transmitting in the 1080i format, the sub channel number should be one.

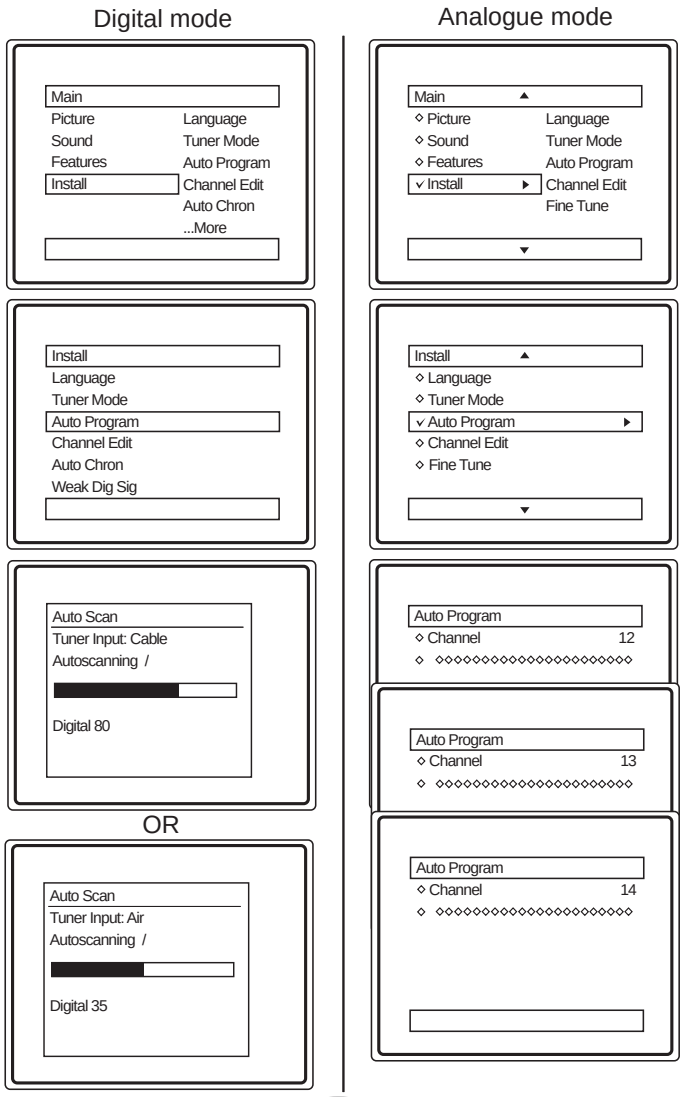


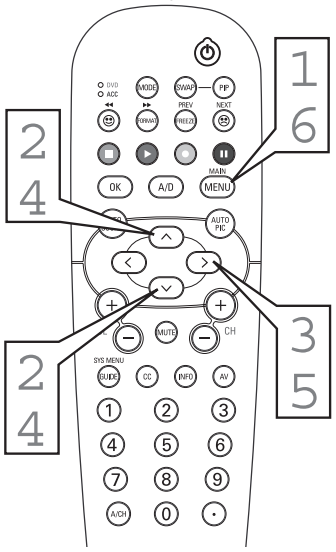
Rear input jacks



This page shows the channel install menus. Note that there are different menus in the Digital and Analog modes.

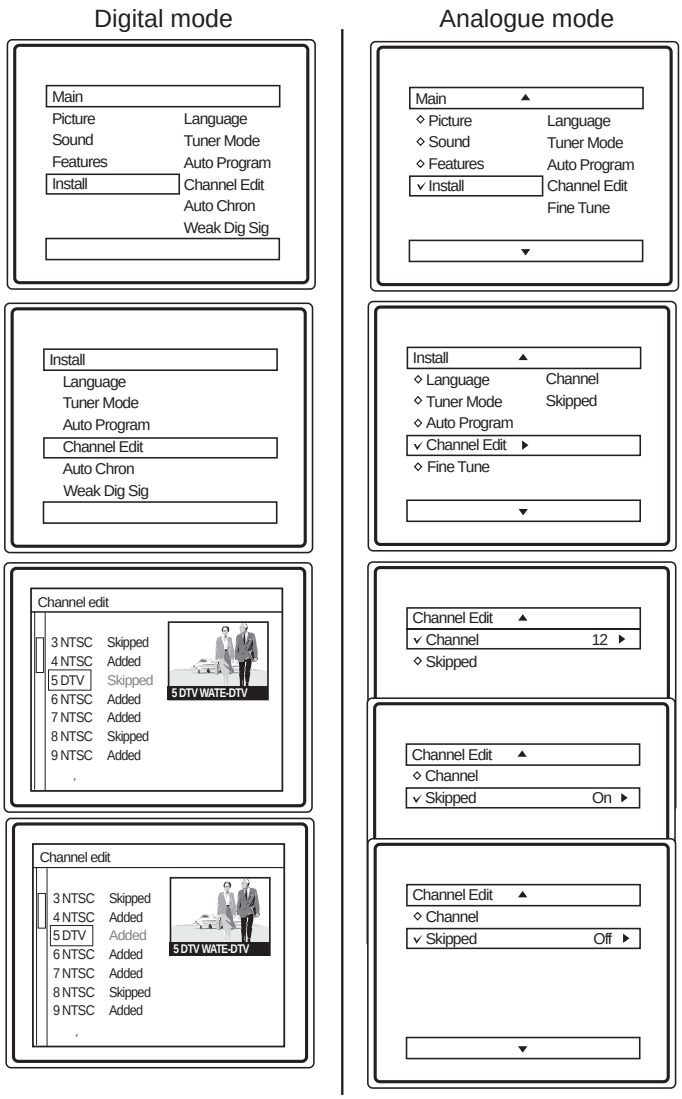
The Digital mode in most cases will require 20 to 40 minutes to install the channels.

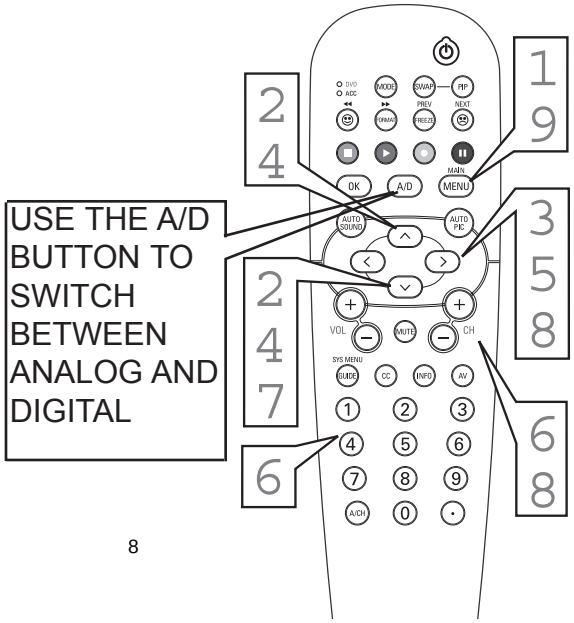




This shows how to edit channels in both the Digital and Analog modes.

It is necessary to have the remote control to switch between the Digital and Analog mode.





Power Supply

Power Supply Block (Figure 14)

Both power supply sections are located on the Family Board. The supplies are divided into two sections, the Auxiliary and Main section. A single filter and rectifier circuit supplies both sections. The Auxiliary supply operates in a low power mode when the load is reduced. In the standby mode, the 3.3 and 6 volt supplies are operating. The 3.3 volt supply provides power to the processor section of the Hercules. The 6 volt supply provides power to the IR receiver. The Main supply is switched Off via the Standby line.

When the set is turned On, the "B" line from the Hercules processor goes High switching 7547 which turns 7535, 7509, and 7545 On. The +3V3A, +6VA, +12VA, and +8VA supplies are then switched On. The load placed on the Aux Power supply will cause it to switch to the full power mode. At the same time, the STBY line switches Low turning the Main SMPS supply On. The supply produces a +6 volt, +140 volt, -16 volt, and +16 volt supplies.

The +Vaudio (+16 volt) supply switches on the degauss relay.

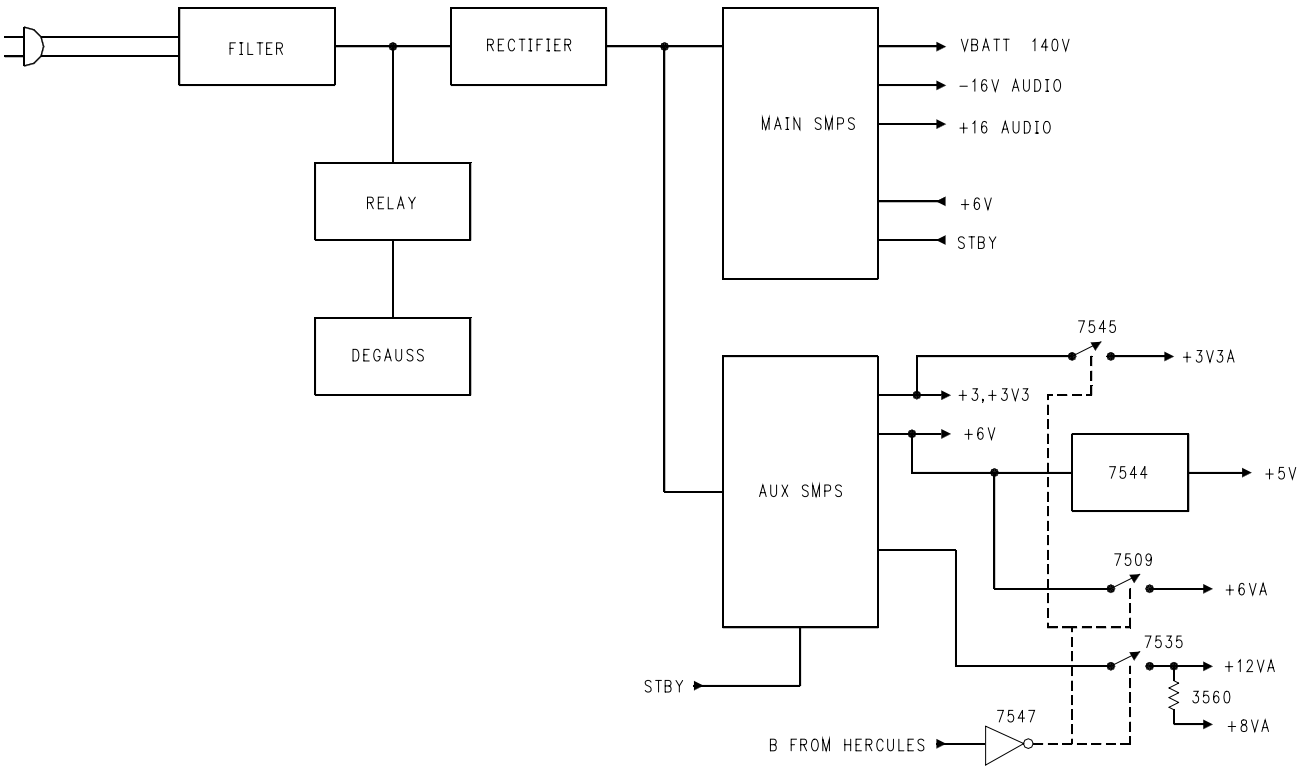


FIGURE 14 - POWER SUPPLY BLOCK

Auxiliary Power Supply (Figure 15)

IC 7510 is the heart of the Auxiliary Power supply. In the Standby mode, VIA the current sensing and Control circuits, a low power condition is detected by the IC. The IC then goes into a Burst Mode operation to reduce the power used by the circuit. In the Burst Mode, the supply will operate at approximately 25 kHz. In full power operation the frequency will be approximately 66 kHz.

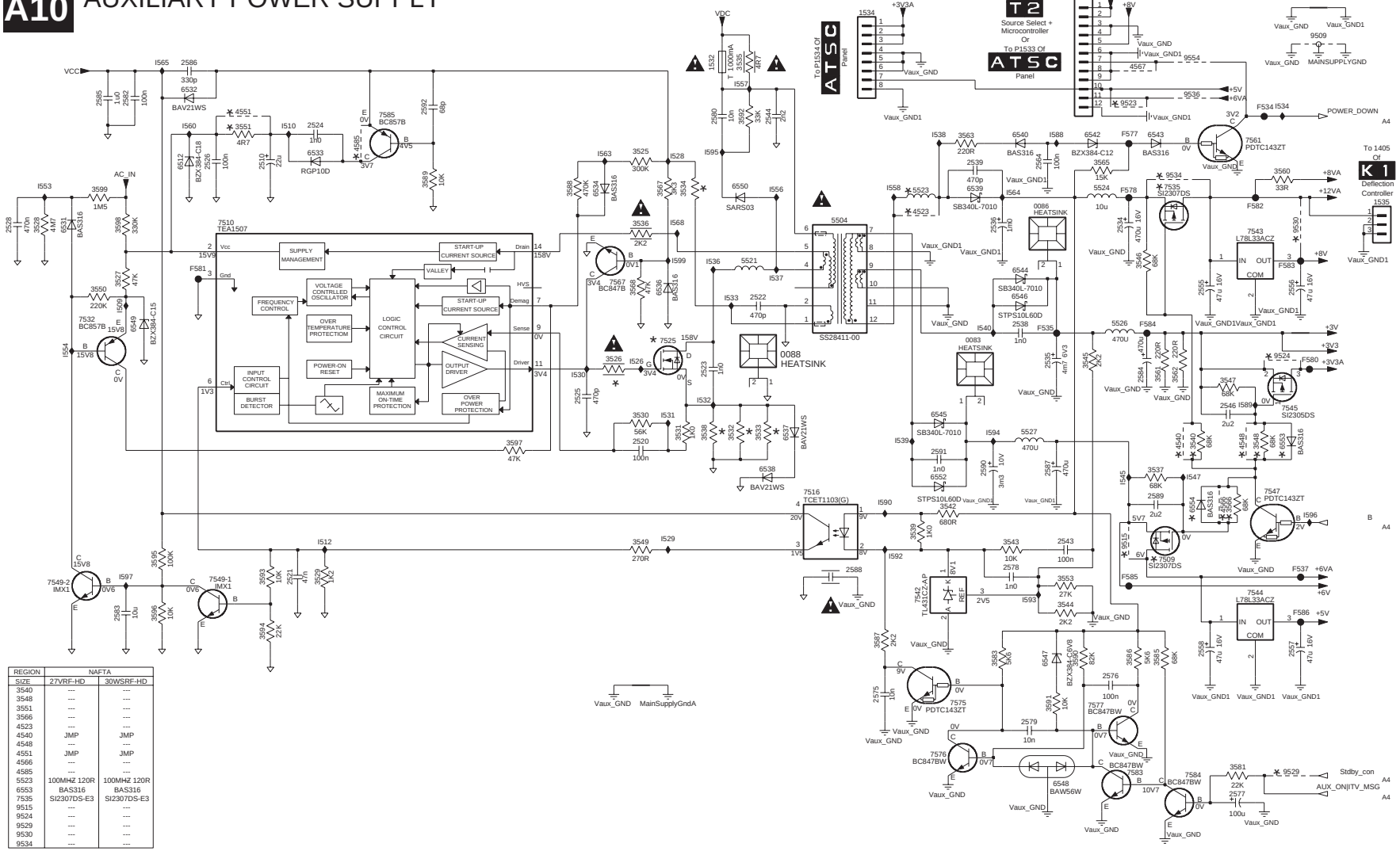
When power is first applied to the set, Start up is supplied to the IC by the internal Start-Up current through Pin 14. Startup voltage is also applied to the IC to Pin 2 by the AC_IN line which is tied to the neutral side of the AC line. During normal operation, power is supplied to the IC by the HOT windings, Pins 1 and 2, of transformer 5504. Output drive from Pin 11 is applied to the Gate of Transistor 7525. Voltage developed across the current sensing resistors in the Source of 7525 provides current sense information to the IC. When 7525 is switched Off, the voltage on Pin 1 of 5504 goes High. This winding supplies the operating voltage the power supply circuit. It also turns Transistor 7567 On causing the Gate of 7525 to stay Low as long as Pin 1 of 5504 is High. This prevents 7525 from turning On until the field of 5504 has collapsed.

Regulation is accomplished by monitoring the +3 volt supply. This voltage is fed to Shunt regulator 7542 which controls the current through opto-isolator 7516. Shunt Regulator 7542 begins conducting when Pin 3 of the IC reaches 2.5 volts. At this point current flows through the opto-isolator, 7516. The transistor inside 7516 turns On applying a control voltage to Pin 6 of 7510. If a problem should develop in the feedback circuit causing an excessive voltage on Pin 6, Transistor 7549-2 will turn On, switching Transistor 7532 On. This will a voltage to the Demag circuit on Pin 7 causing the IC to latch Off. The IC will stay latched until power is removed and reapplied to the set.

In the Standby mode, the "B" control line from the Hercules Processor is Low. Only the +3, +3V3, and +6 volt supplies are present. When the set is turned On, the "B" line will go High, turning Transistors 7509, 7545, and 7535 On. This will switch On the +8VA, +12VA, +8V, +3V3A, +6VA, and +5V supplies.

In normal operation, voltage from Pin 12 of 5504 is rectified by 6540 to produce a negative voltage which prevents Transistor 7561 from turning On. If AC is removed from the set, this negative voltage will disappear. The voltage across the filter capacitors on the +3V line will turn 7561 On. The Power Down line will then go Low signaling the processor to shut the set down.

A10 AUXILIARY POWER SUPPLY



REGION	NAFTA	
SIZE	27VRF-HD	30WSRF-HD
3540	---	---
3548	---	---
3551	---	---
3566	---	---
4523	---	---
4540	JMP	JMP
4548	---	---
4551	JMP	JMP
4566	---	---
4585	---	---
5523	100MHZ 120R	100MHZ 120R
6553	BAS316	BAS316
7535	SI2307DS-E3	SI2307DS-E3
9515	---	---
9524	---	---
9529	---	---
9530	---	---
9534	---	---

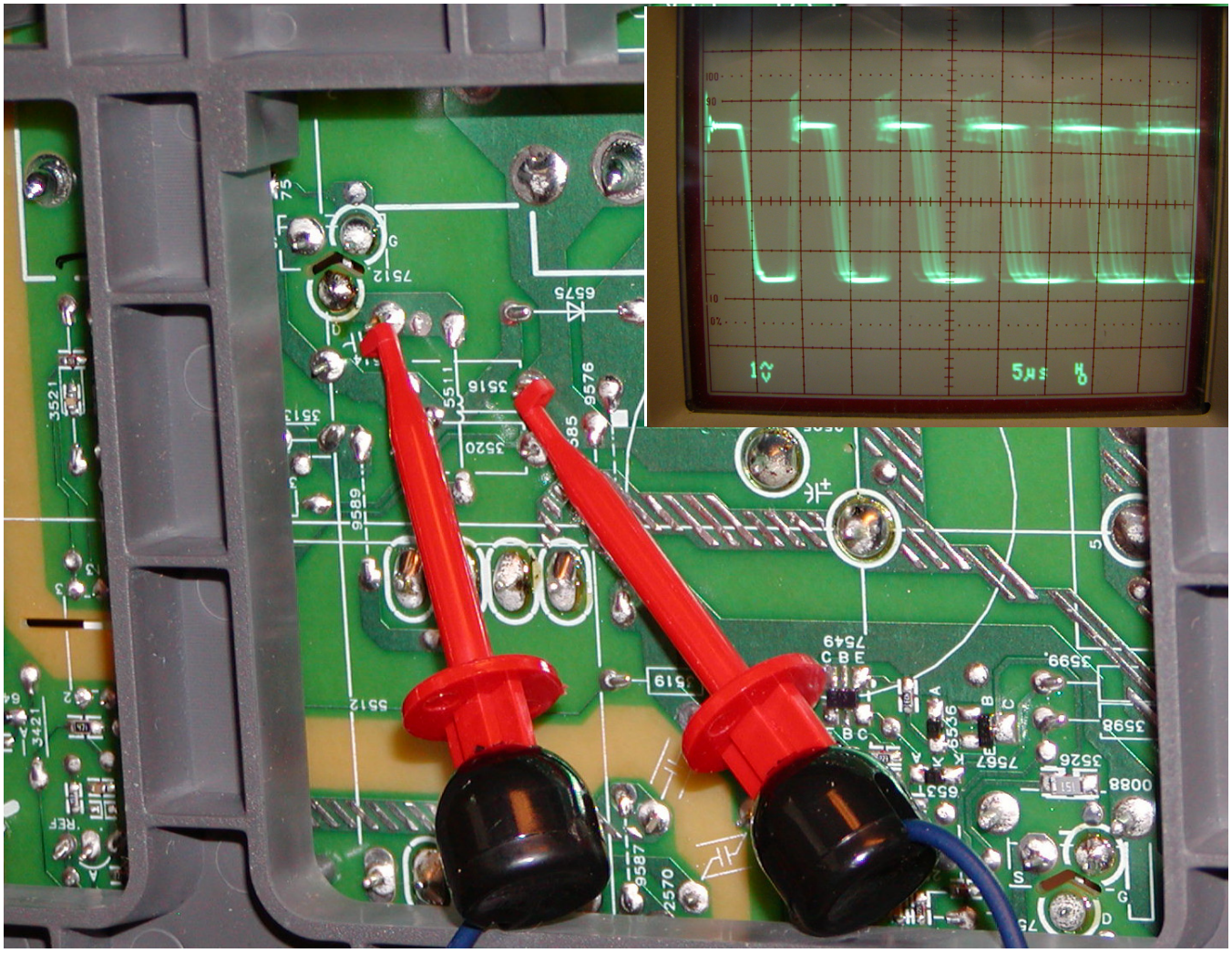
Main power supply (Figure 16)

The Main Power supply provides the VBAT (141 volt), and Audio voltage supplies. This supply is switched Off during the Standby mode. During Standby the STBY_Con line is High which turns Transistor 7573 On. This causes the opto-isolator 7513 to turn On hard. This places a higher voltage on the control Pin of IC 7511 causing the IC to shut down. The operating voltage from the Auxiliary supply keeps a small voltage on Pin 2 of 7511 to prevent it from cycling On and Off.

When the set is turned On, the STBY_Con line goes Low switching 7573 Off. The VBAT supply is the reference voltage for regulation. Since this voltage is missing during startup, the Shunt Regulator 7571 is turned Off. The voltage on Pin 6 of 7511 goes Low, which turns the drive from the IC On. When the set is On during normal operation, the supply voltage on Pin 2 of the IC is supplied by Pin 2 of Transformer 5512. When the VBAT supply reaches the correct voltage, Pin 3 of the Shunt Regulator 7571 reaches 2.5 volts switching it On. This switches the opto-isolator On to provide a regulation feedback path.

Transistor 6551 provides a power on ramping of the VBAT supply.

Power FET drive points



A1 POWER SUPPLY

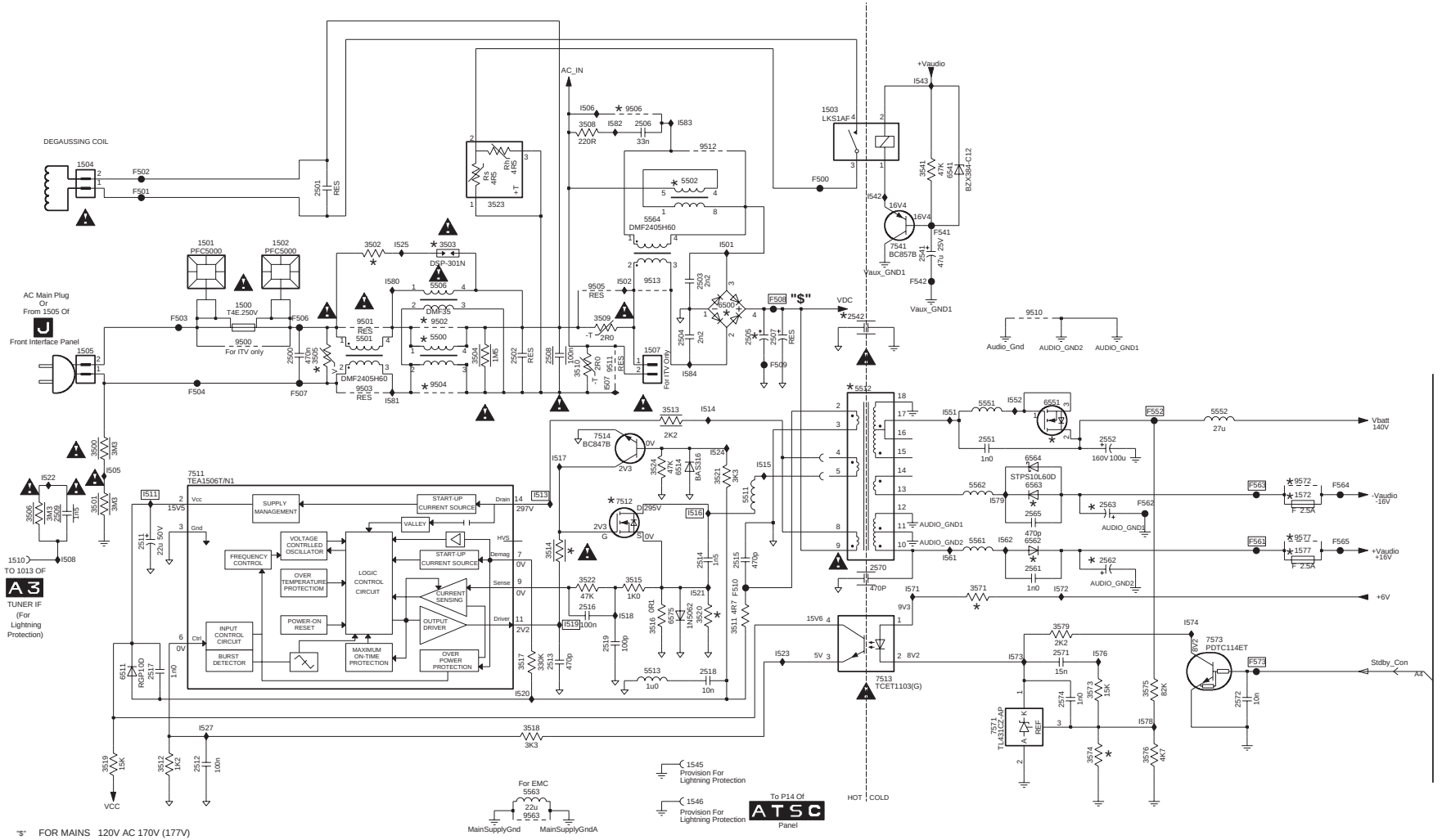


FIGURE 16 - MAIN POWER SUPPLY

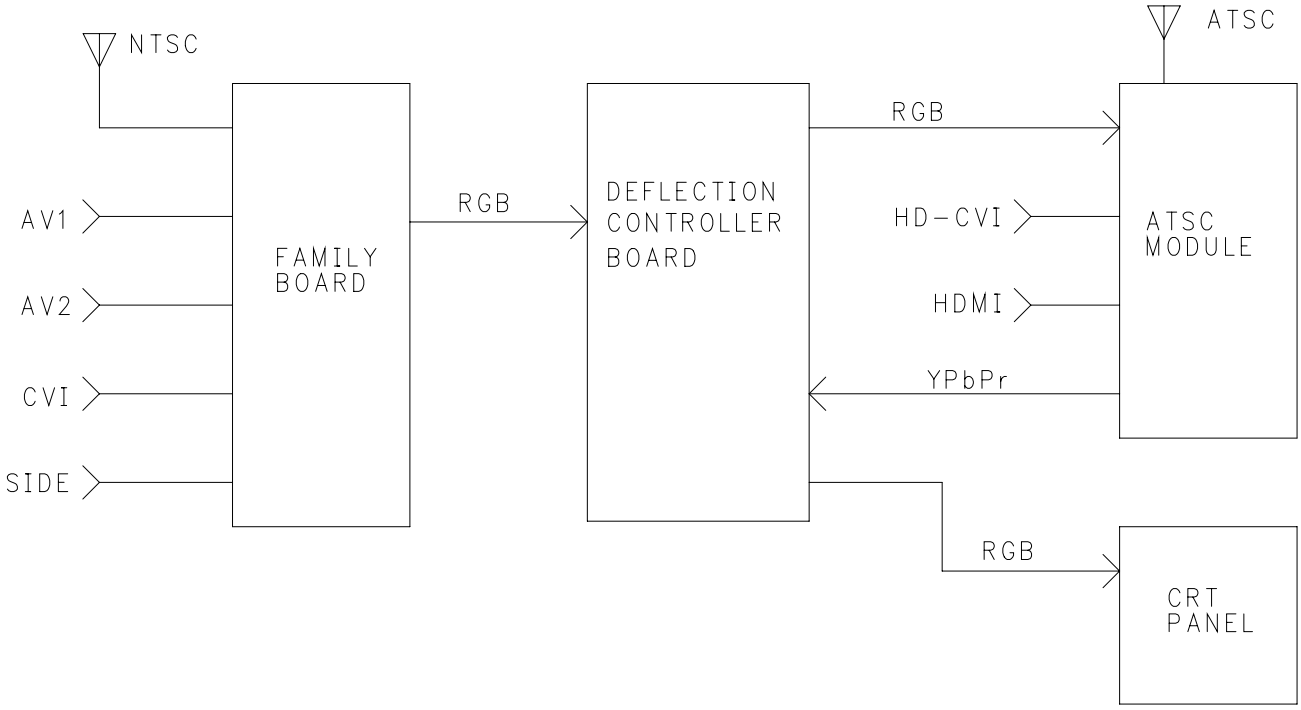


FIGURE 17 - OVERALL VIDEO SIGNAL FLOW BLOCK

Video Signal Flow

Overall Block (Figure 17)

The video processing section located on the Family Board (Mono Carrier board) performs all of the 1fH processing. AV1, AV2, CVI, and Side inputs are fed to this board. The CVI input on this board will only accept 1fH signals. 1fH RGB signals from the Family board is fed to the Deflection board and then to the ATSC module. The ATSC module rescales the picture from the Family board. It also has an HDMI and CVI connection. The HDMI and CVI connections can accept either 480i, 480p, 720p, or 1080i. The ATSC module also has a built in Digital Tuner. The ATSC module resizes the picture to 1080i regardless of the input.

The YPbPr output of the ATSC module is fed to the Deflection Controller board for video processing and deflection control. RGB from the Deflection Controller board is fed to the CRT panel.

Customer adjustments such as Brightness, Contrast, Color, and Tint are performed on the Deflection Processor panel.

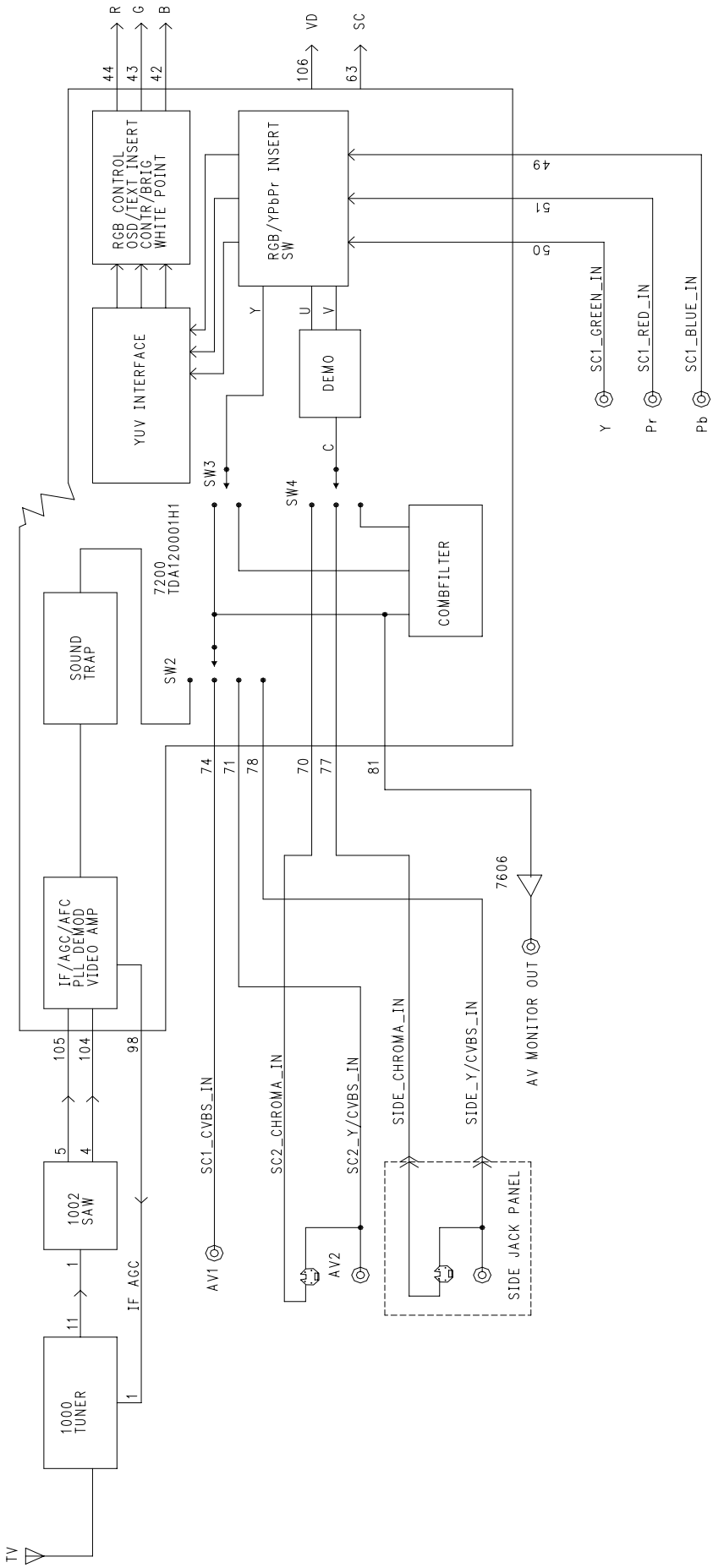


FIGURE 18 - FAMILY BOARD VIDEO PROCESSING

Family Board Video Processing (Figure 18)

Video processing on the Family board is performed by IC 7200, Hercules. IF from the NTSC Tuner, 1000, is fed to SAW filer 1002 and then to 7200. The demodulated video is fed to an internal switch which selects between the Tuner video, AV1, AV2, or the Side Jack panel. Monitor video is output on Pin 81. There is no monitor out for the ATSC section. The video is fed to an internal Comb filter to separate the Luminance and Chrominance, YC. The Chroma is fed to the Color Demodulator and to the YUV switch along with the Luminance. The YUV switch selects between the internal demodulated signal and the YPbPr signal. This is a 1fH only input.

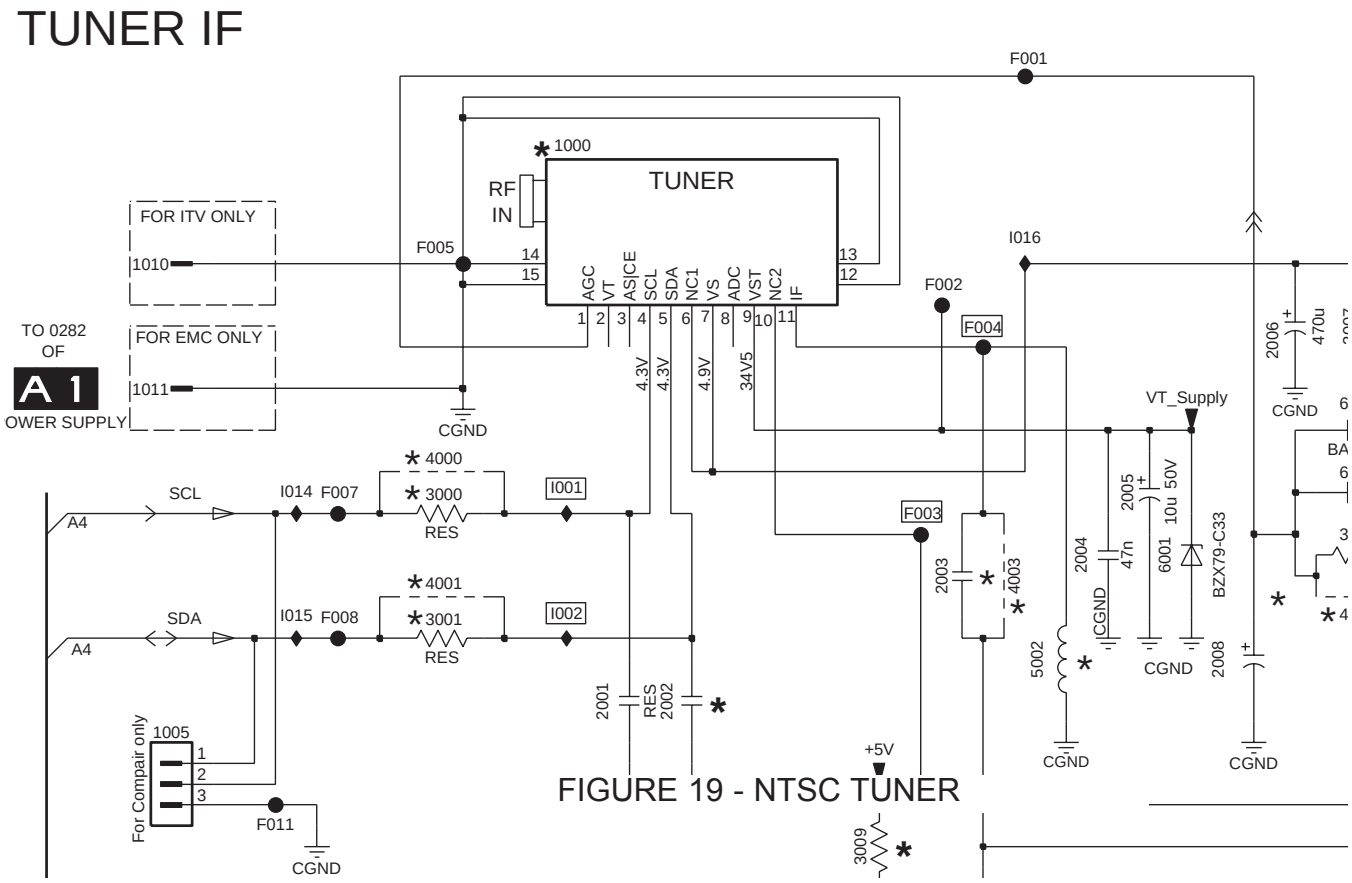


FIGURE 19 - NTSC TUNER

NTSC Tuner (Figure 19)

The Tuner for the NTSC signals is located on the Family board. The VT_Supply is derived from the VBat supply. It is regulated to 33 volts by zener diode 6001. The Tuner is controlled by the I2C bus from the Hercules processor.

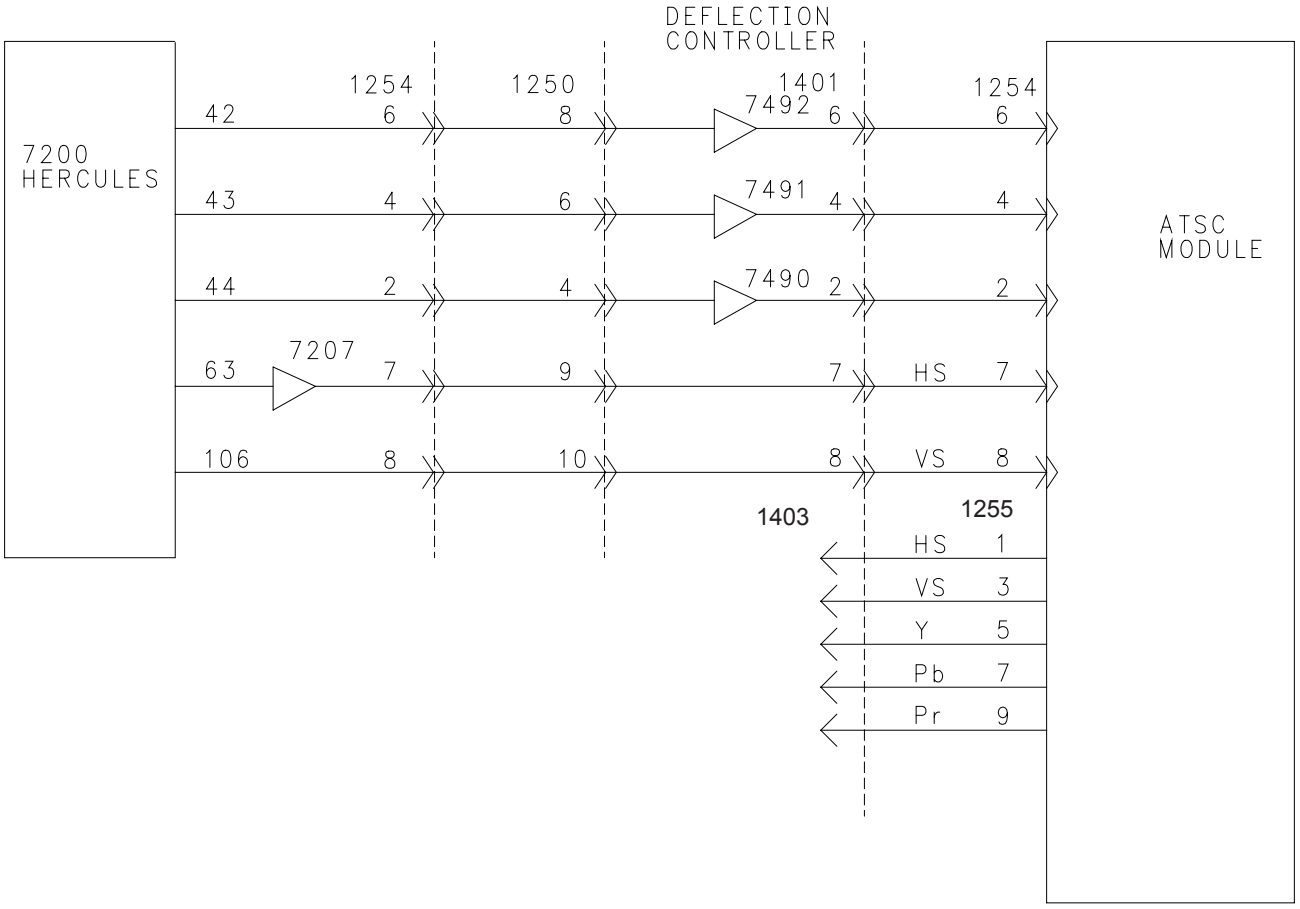


FIGURE 20 - VIDEO TEST POINTS

Video Test Points (Figure 20)

The connection points between modules can provide test points to determine which circuit board requires repair or replacement. The RGB and Sync signals from the Hercules is fed to the Deflection Controller board on connector 1254. These signals are buffered by transistors 7492, 7491, and 7490 before being fed to the ATSC module on connectors 1401 and 1254. After the signal is processed, it is fed back to the Deflection panel on connectors 1255 and 1403. Refer to the wiring interconnect diagram for additional check points.

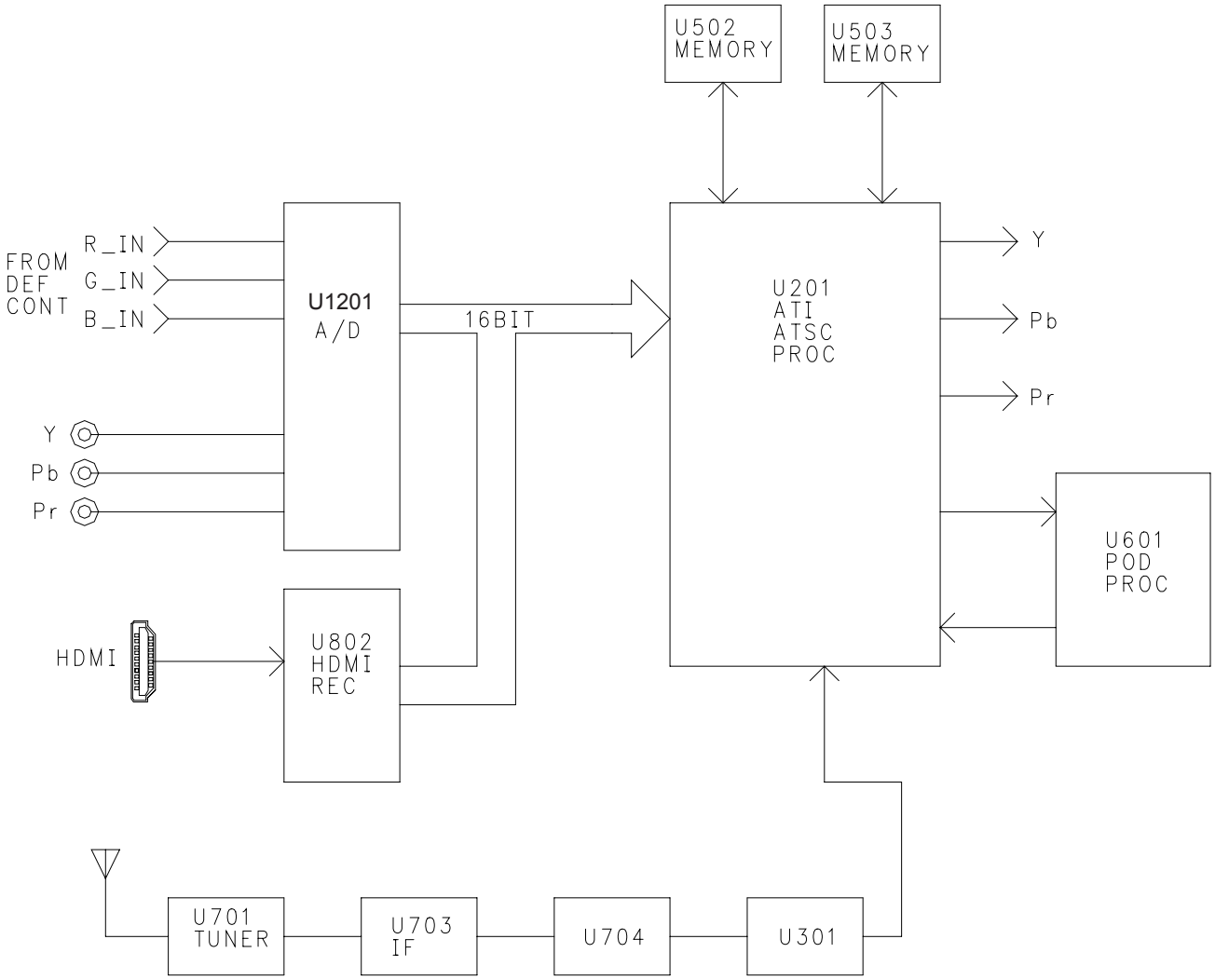


FIGURE 21 - ATSC BLOCK

ATSC Block (Figure 21)

RGB from the Deflection module and Component video from the YPbPr input if fed to U1201, switch. The YPbPr input on the ATSC module can be 480i, 480p, 720p, or 1080i. The A/D, U201 shares a 16bit bus with the HDMI receiver. The Customer selected signal is fed to U201, the ATSC processor. The ATSC processor enhances and rescales the signals from these inputs. The ATSC tuner, U701, is fed to the IF section, U703, and then to filters U704 and U703. The ATSC processor can decode either 8VSB terrestrial, 64QAM, or 256QAM signals.

The output of the ATSC processor is fed to the POD processor IC. Most of the POD processing circuit is not present since this set does not have that feature. Two memory ICs, U502 and U503 stores the picture information while the video is being processed. The analog YPbPr 1080i signals are output to the Deflection panel.

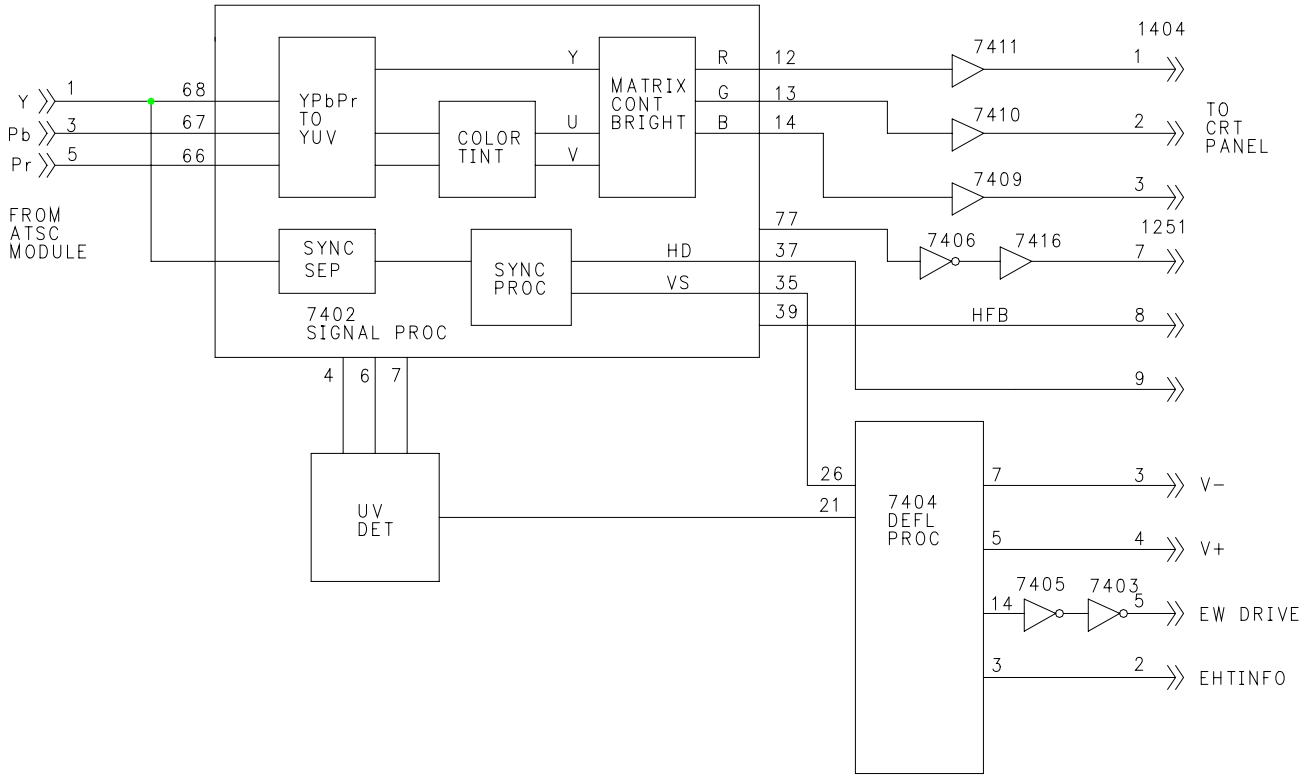


FIGURE 22 - DEFLECTION BLOCK

Deflection Panel Block (Figure 22)

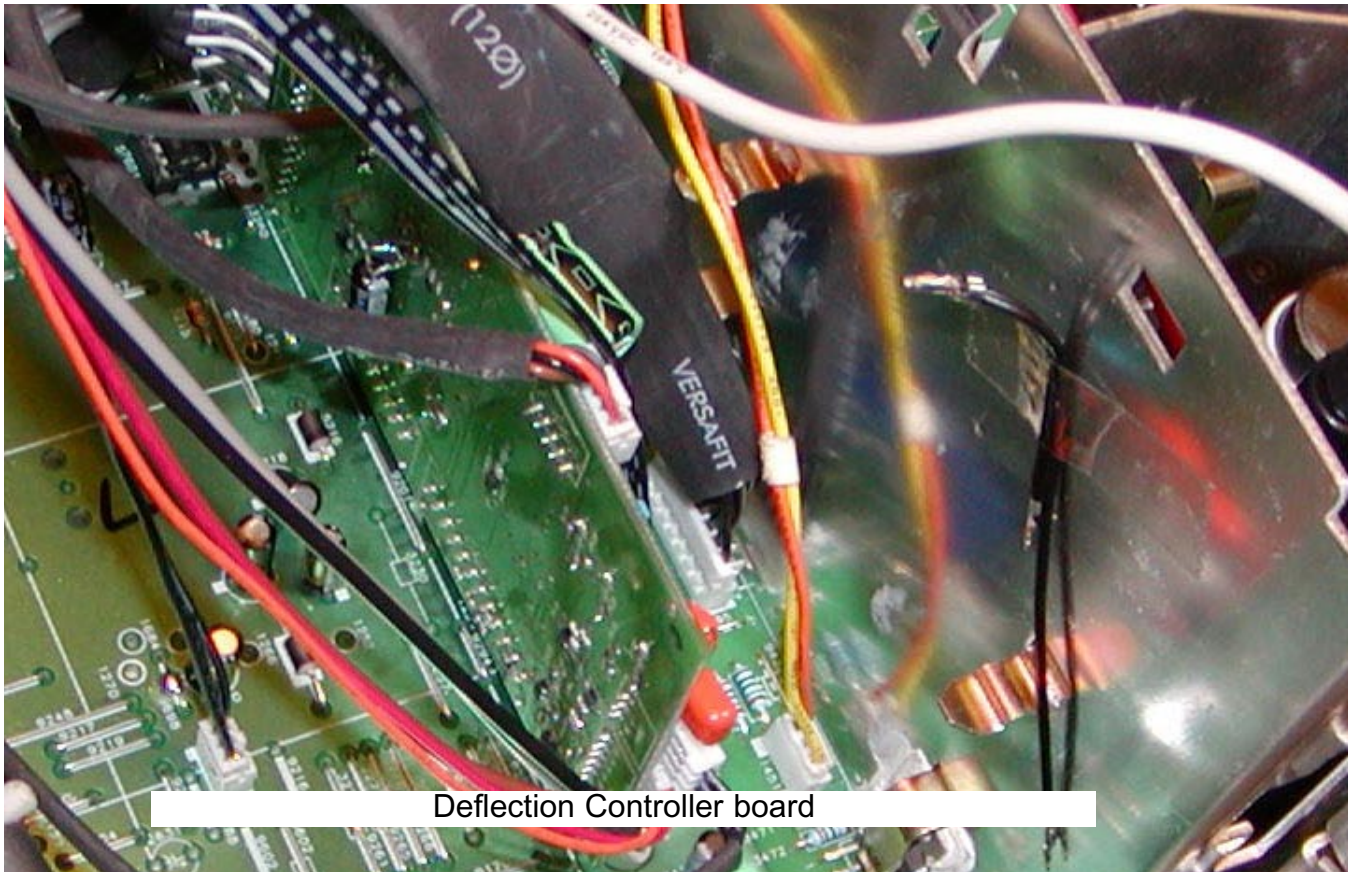
The Deflection panel performs the signal processing and Deflection processing functions. YPbPr from the ATSC module is fed to 7402 signal processor. This circuit performs the Color, Tint, Brightness, and Contrast control functions. The Y signal is fed to a Sync Separator to separate the Horizontal and Vertical Sync which is output on Pins 37 and 35. RGB is output on Pins 12, 13, and 14. These signals are sent to the CRT panel.

Horizontal drive is output on Pin 37 where it is fed to the deflection circuits on the Family board. Vertical Sync is output on Pin 35 of 7402 to IC 7404. IC 7404 develops the Vertical and EW drive for the deflection circuits.

DC monitor signals are output on Pins 4, 6, and 7 of 7402 and fed to an Under voltage detection circuit. If a positive or negative voltage develops on any of these lines, this circuit will force Pin 21 of 7404 Low, causing the set to shut down. The shutdown is activated when Pin 21 goes below 5 volts.

CRT board

As shown in figure 23, the Filament voltage, 200 volt, 8 volt, and 12 volt supplies are fed to the CRT panel on connector 1351. The 141 volt supply powers the SCAVEM.



Deflection Controller board

Deflection (Figure 23)

Horizontal drive from 7221 is fed to Transistor 7404 located on the Family board. This drive circuit has two power sources. During startup, it is powered by the +6 volt supply. Once the High Voltage circuit is running, it is powered by Pin 9 of the IFT. 7404 drives Transformer 5402 which drives the HOT (Horizontal Output Transistor). The HOT drives the IFT and the Horizontal Deflection Coil. The IFT is powered by the VBAT (141 volt) supply.

The IFT produces High voltage, Focus voltage and G2 voltage to drive the CRT. In addition, a 200 volt supply is produced to drive the CRT panel, a +14 and -14 volt supply for the Vertical output, Filament voltage, +200 volt VideoSupply, and a +12V_Iot supply.

Transistor 7408 monitors the IFT secondary to sense the presence of over voltage. If the High Voltage goes High, the voltage on Pin 6 of the IFT will go High. When the voltage on diode 6480 exceeds 15 volts, transistor 7408 will turn On. If 7408 turns On, it will turn 7407 On causing the x_ray protect line to go Low. The Processor will then shut the set down. In addition the EW_DRIVE circuit is monitored. If the EW_DRIVE fails, transistor 7406 will turn On constantly placing a dc voltage on the source. This will turn 7407 On.

IC 7451 is the Vertical Output IC. It is powered by the +14 and -14 volt supply from the IFT. The Vertical pulse is rectified by 6458, keeping the V_PROTN line High. If the vertical output should fail, the V_PROTN line will go Low. The Hercules processor will then shut the set down.

A2 LINE + FRAME DEFLECTION

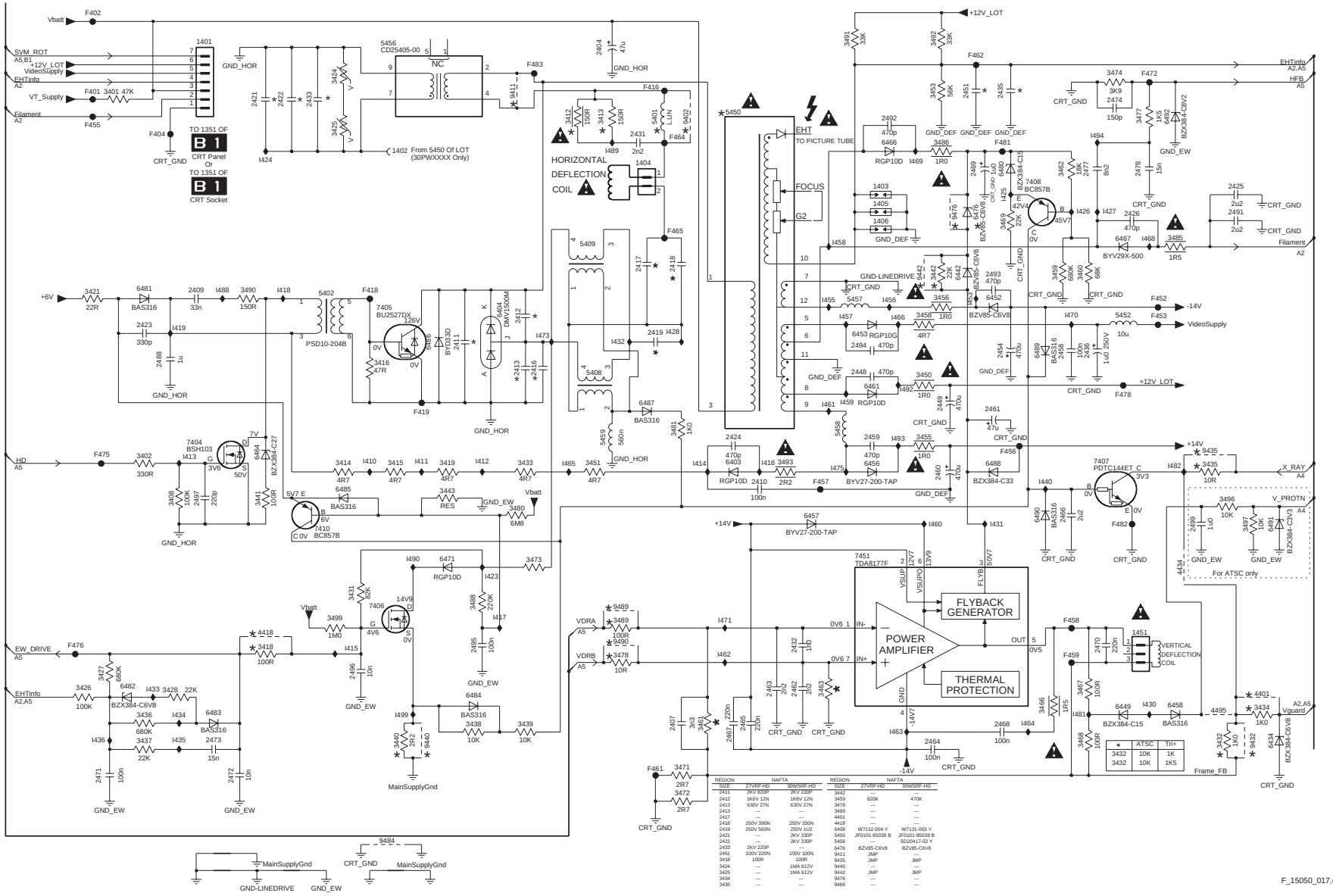


FIGURE 23 - DEFLECTION

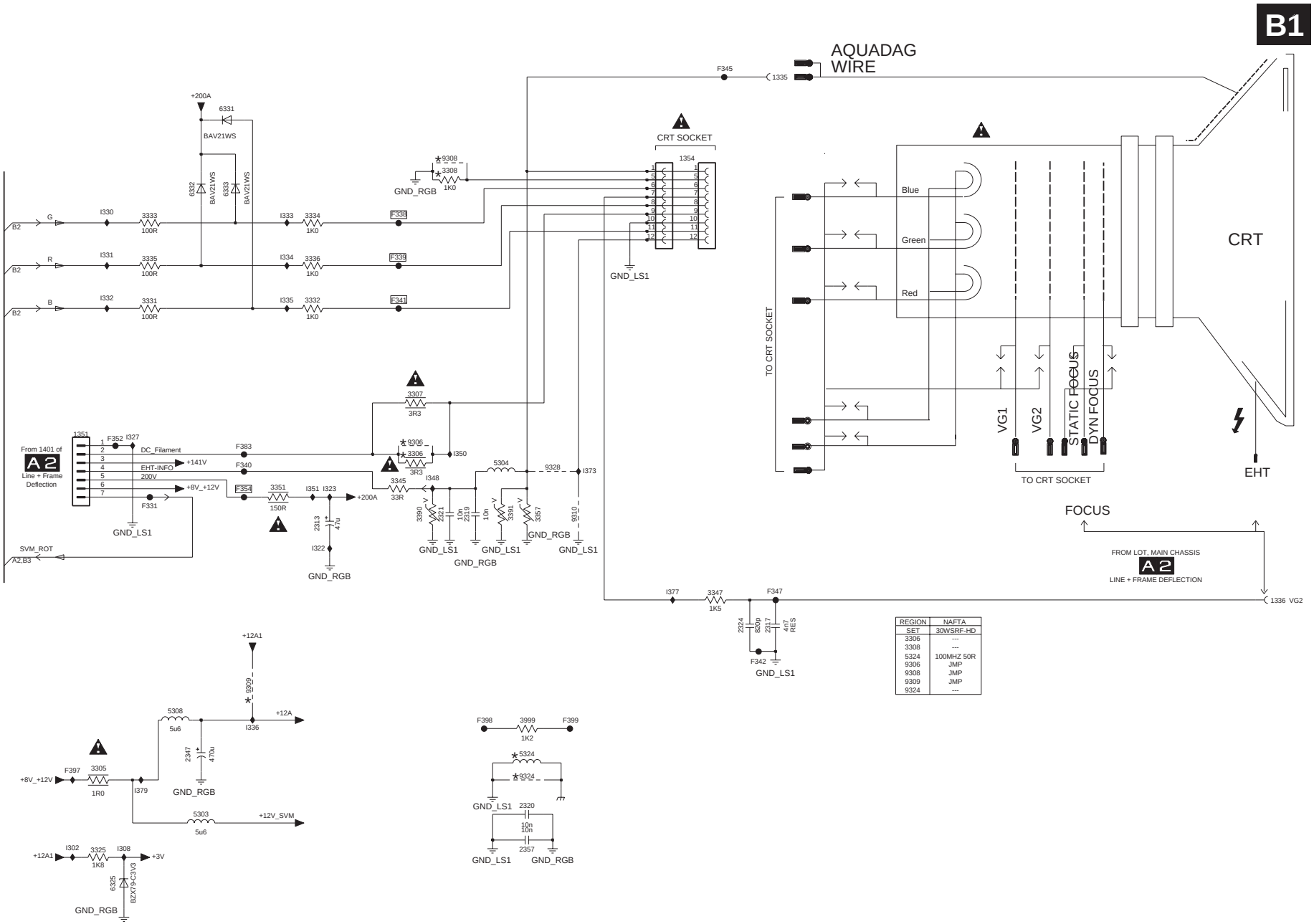


FIGURE 24 - CRT

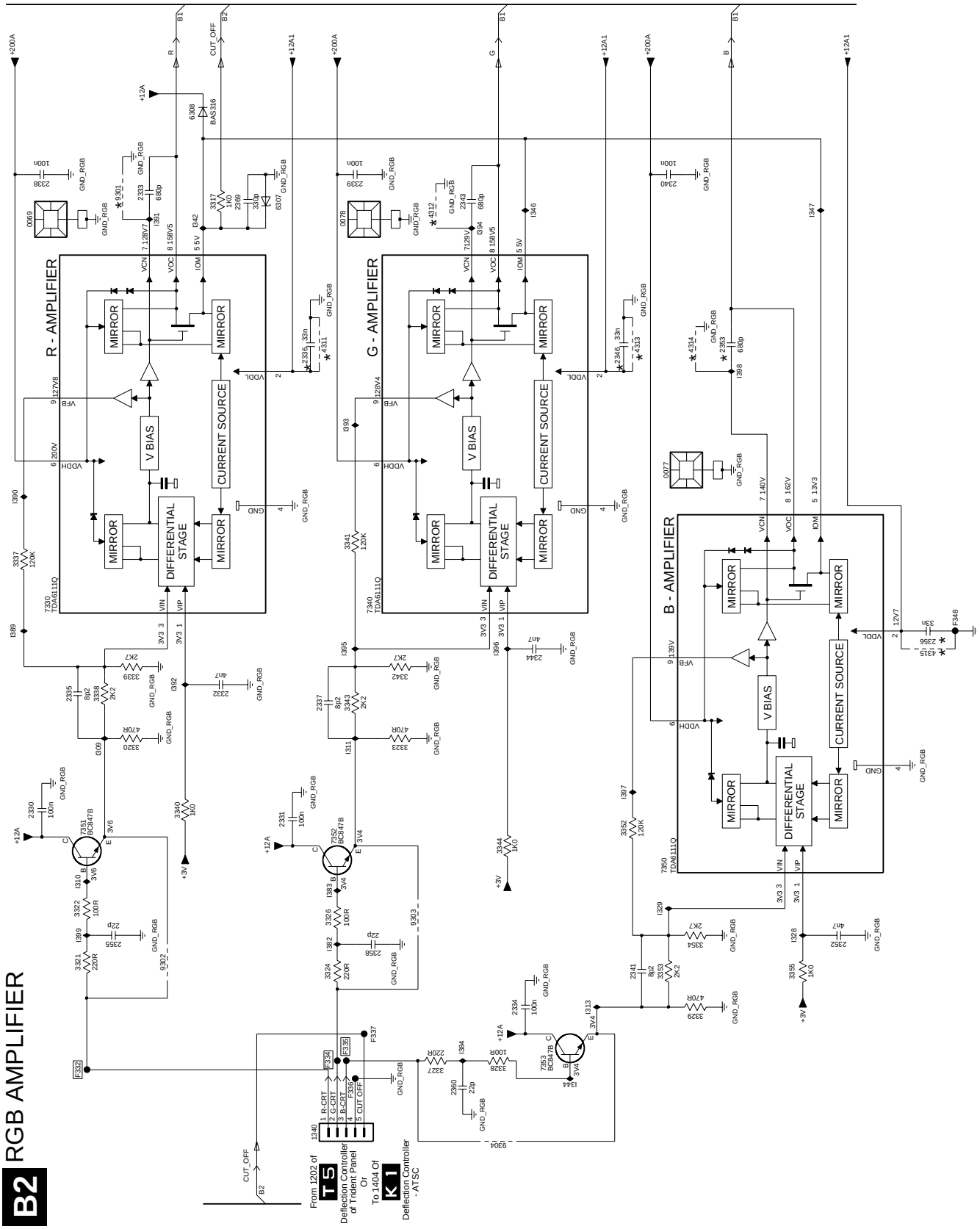


FIGURE 25 - CRT DRIVE

ROTATION & SCAVEM

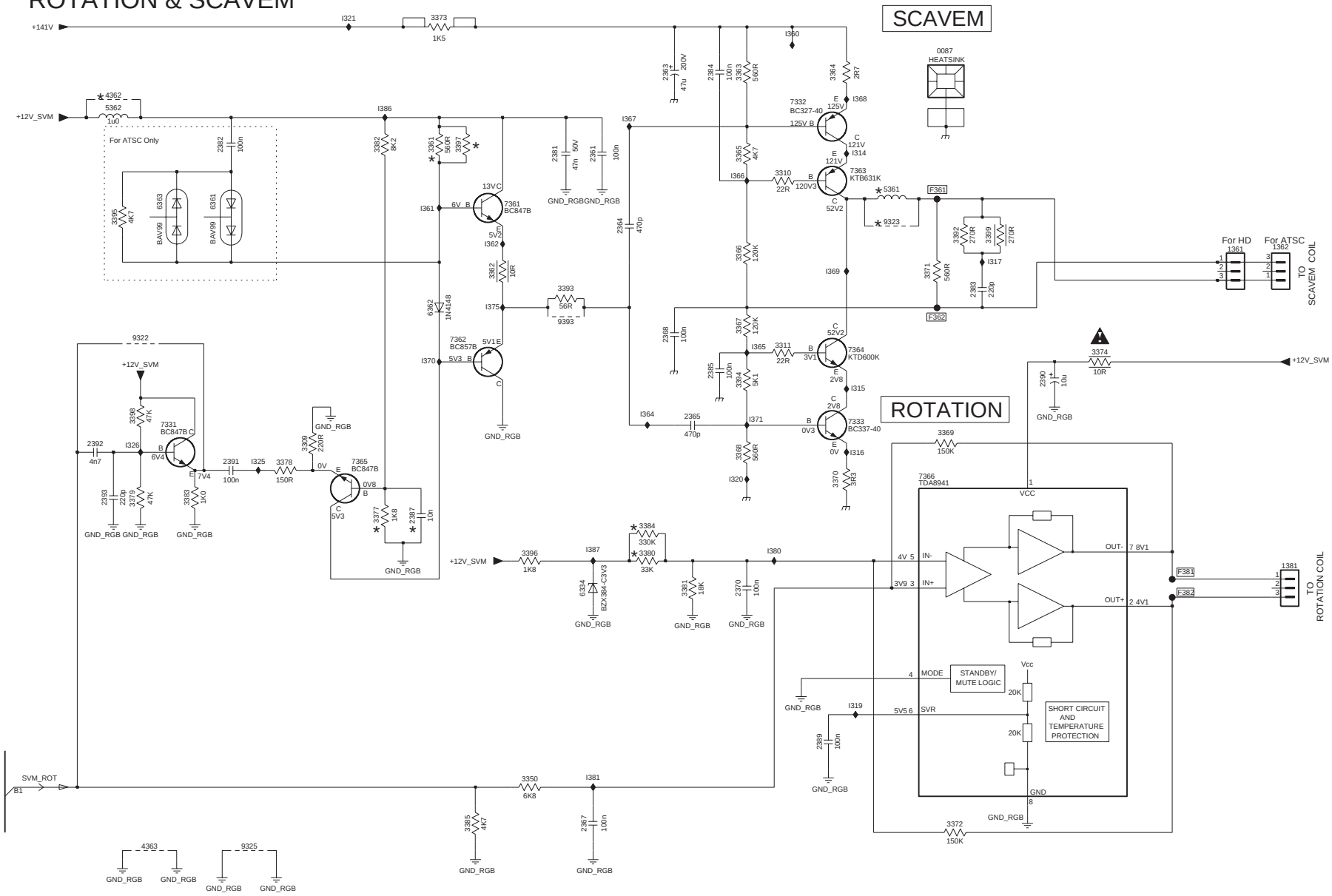


FIGURE 26 - SCAVEM AND ROTATION

CRT Drive (Figure 25)

RGB drive is fed to the CRT board on connector 1340 to transistors 7351, 7352, and 7353. The signal is then fed to the three CRT drive amplifier ICs, 7330, 7340, and 7350. These amplifiers are powered by the 200 volt supply.

SCAVEM and Rotation (Figure 26)

The Rotation and SCAVEM (SCAn VElocity Modulation) signals are both on the SVM_ROT line. The Rotation signal is a low frequency signal. The high frequency is filtered out by capacitor 2367. The Rotation signal is blocked by capacitor 2391.

The Rotation signal is amplified by 7366. A four transistor output circuit drives the SCAVEM coil.

Audio

Family board audio input (Figure 27)

NTSC IF for audio, Side input, AV1, and AV2 are fed to the Hercules, 7200. The selected audio is output on Pins 66 and 67 and fed to the ATSC module. Audio demodulation for NTSC in done in the Hercules.

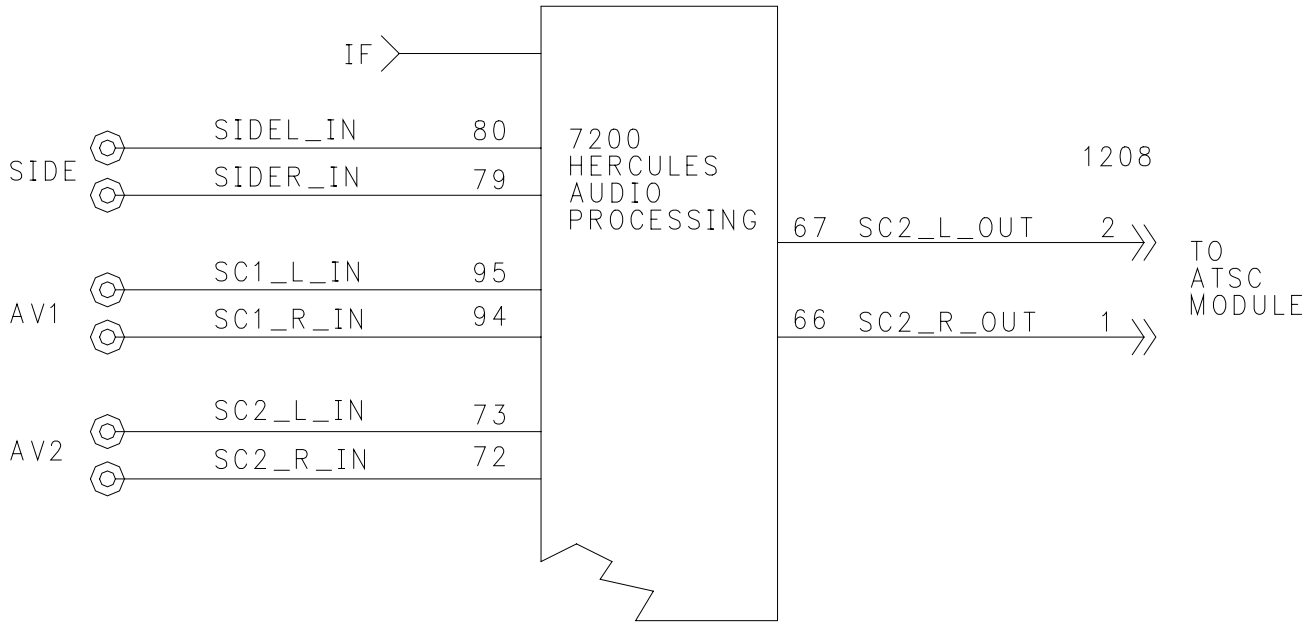


FIGURE 27 - FAMILY BOARD AUDIO INPUT

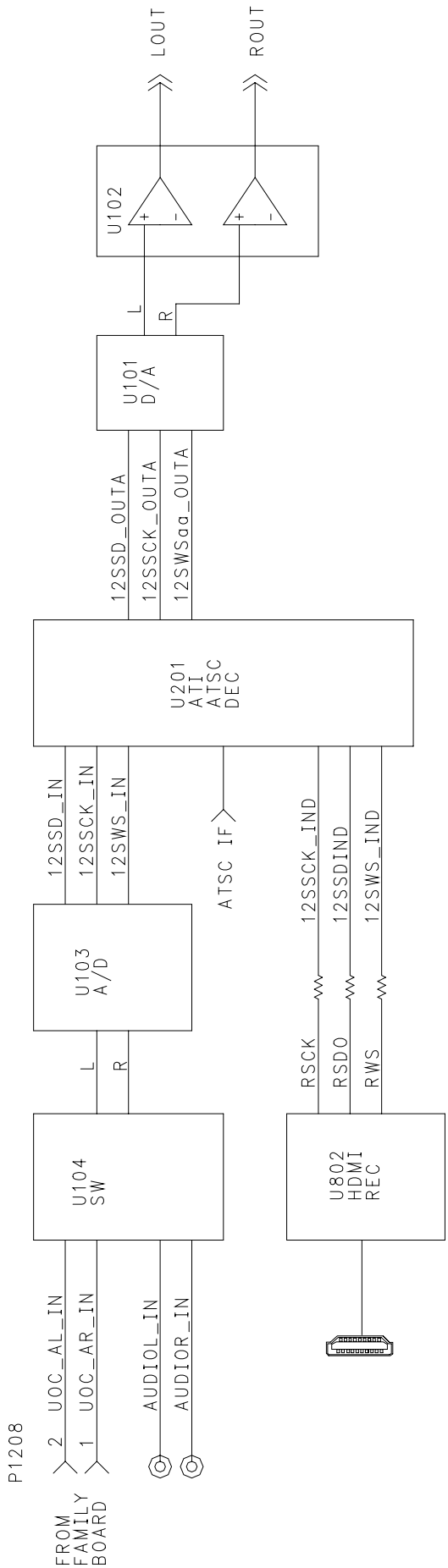


FIGURE 28 - ATSC Audio Block

ATSC Audio Block (Figure 28)

All of the audio in the set is routed through the ATSC module. Audio for the HD CVI connection located on the ATSC module and audio from the Family board is fed to switch U104. The selected audio is fed to A/D U103. Digital audio is fed to the ATSC decoder, U201. Digital audio from the HDMI receiver, U802, is also fed to U201. The ATSC decoder selects between the HDMI, Analog inputs or the internal ATSC decoder. After processing, digital audio is output to U101, buffered by U102, and then fed back to the Family board.

Audio Output (Figure 29)

Selected audio output from the ATSC module is fed back to IC 7200, Hercules. The Hercules performs the audio control functions, Volume etc. The audio is then output on Pins 68 and 69 and fed to the audio amplifier, 7990. The audio amplifier is a dual 10 watt amplifier. It is powered by the +VAUDIO and -VAUDIO supplies which are +16 and -16 volts. To mute the amplifier, the VOL_MUTE line goes Low, switching transistor 7992 Off, switching transistor 7991 On. The output of the amplifier is fed to the Side Jack panel.

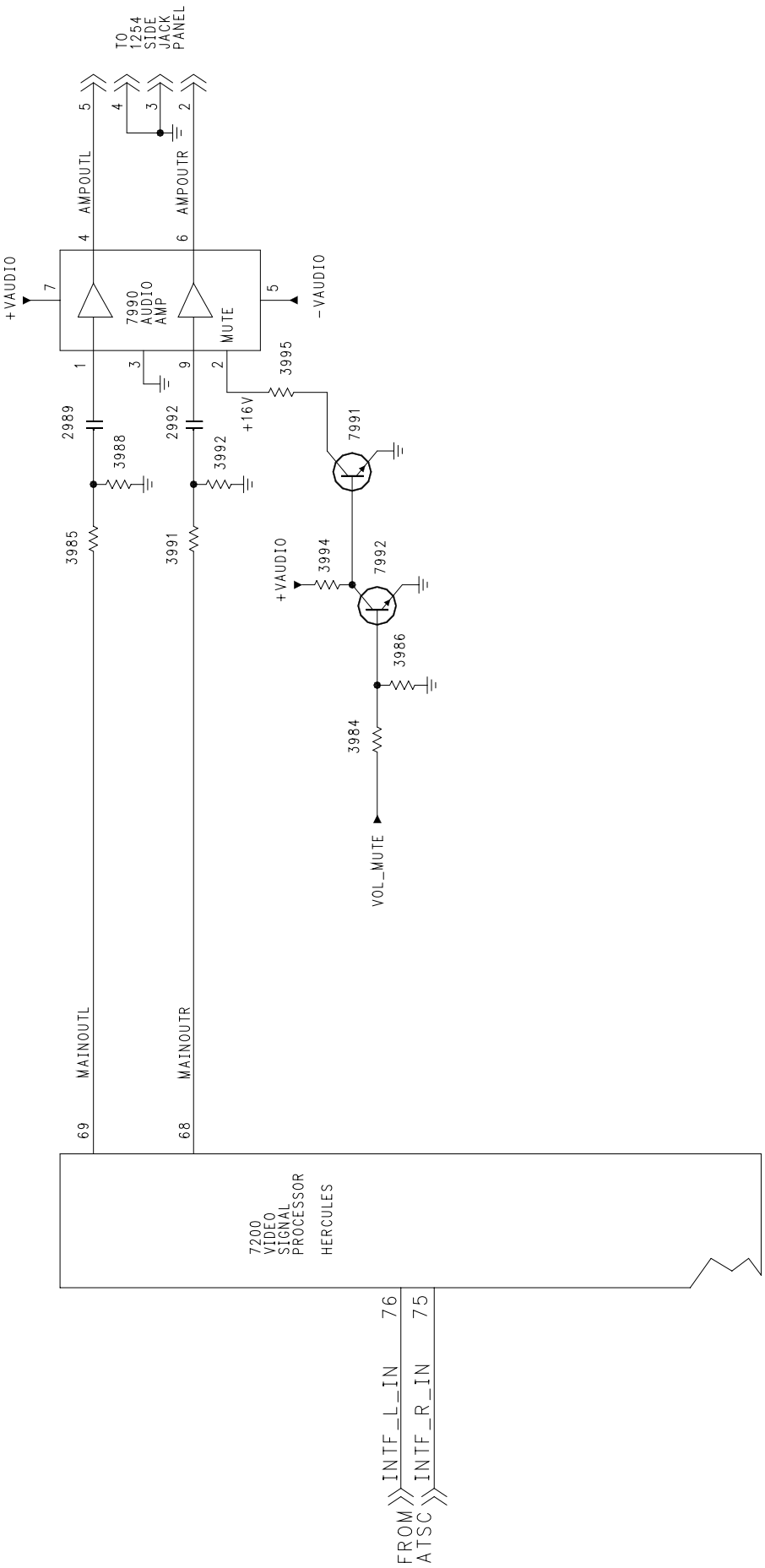


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FIGURE 29 - AUDIO OUTPUT

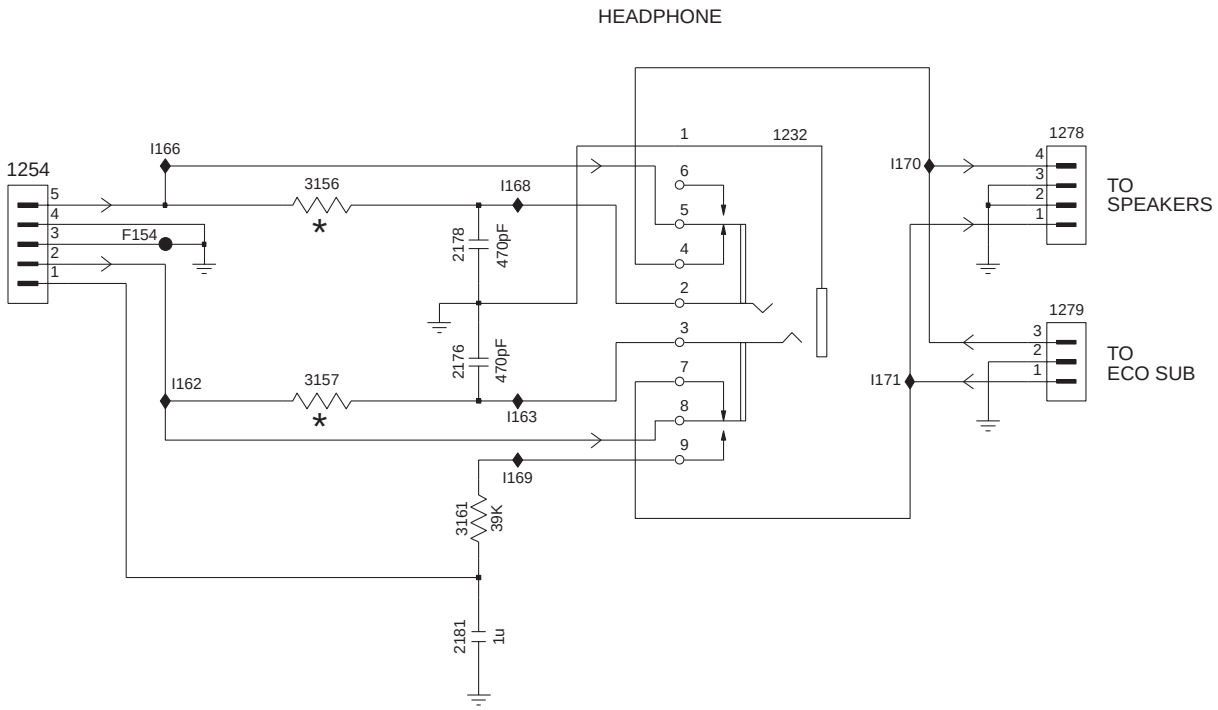

FIGURE 30 - SIDE JACK PANEL

Side Jack Panel (Figure 30)

The output of the audio amplifier is fed to the Headphone Jack located on the Side Jack panel. The output to the speakers is switched Off when the headphone plug is inserted.

Locating the Defective panel (Figure 31)

When troubleshooting the set, the defective panel requiring replacement or additional repair must be located. The Power supplies, Deflection, NTSC Tuning, 1 fH inputs, and Audio output are located on the Family board. The 2 fH inputs, ATSC Tuning, Digital Audio processing is located on the ATSC panel. Video processing and Deflection signal circuits are located on the Deflection Controller panel.

If the set turns On without a picture or sound, first check the Power supplies located on the Family board. If the set comes On, then shuts Off, there may be a problem with the shut-down circuits also located on the Family board. If the picture is missing, but sound is present, switch to an ATSC channel. If the picture returns, the problem is most likely on the Family board. If the picture is still not present, check the YPbPr signals on connector P1255 located on the ATSC module. If video is present at this point, then check the Deflection Controller. Check the RGB out to the CRT panel on connector 1340 on the CRT panel.

If High Voltage is not present when the voltage supplies turn On, check the Horizontal and Vertical drive from the Deflection Controller panel. These signals can be checked on connector 1251 located on the Family board.

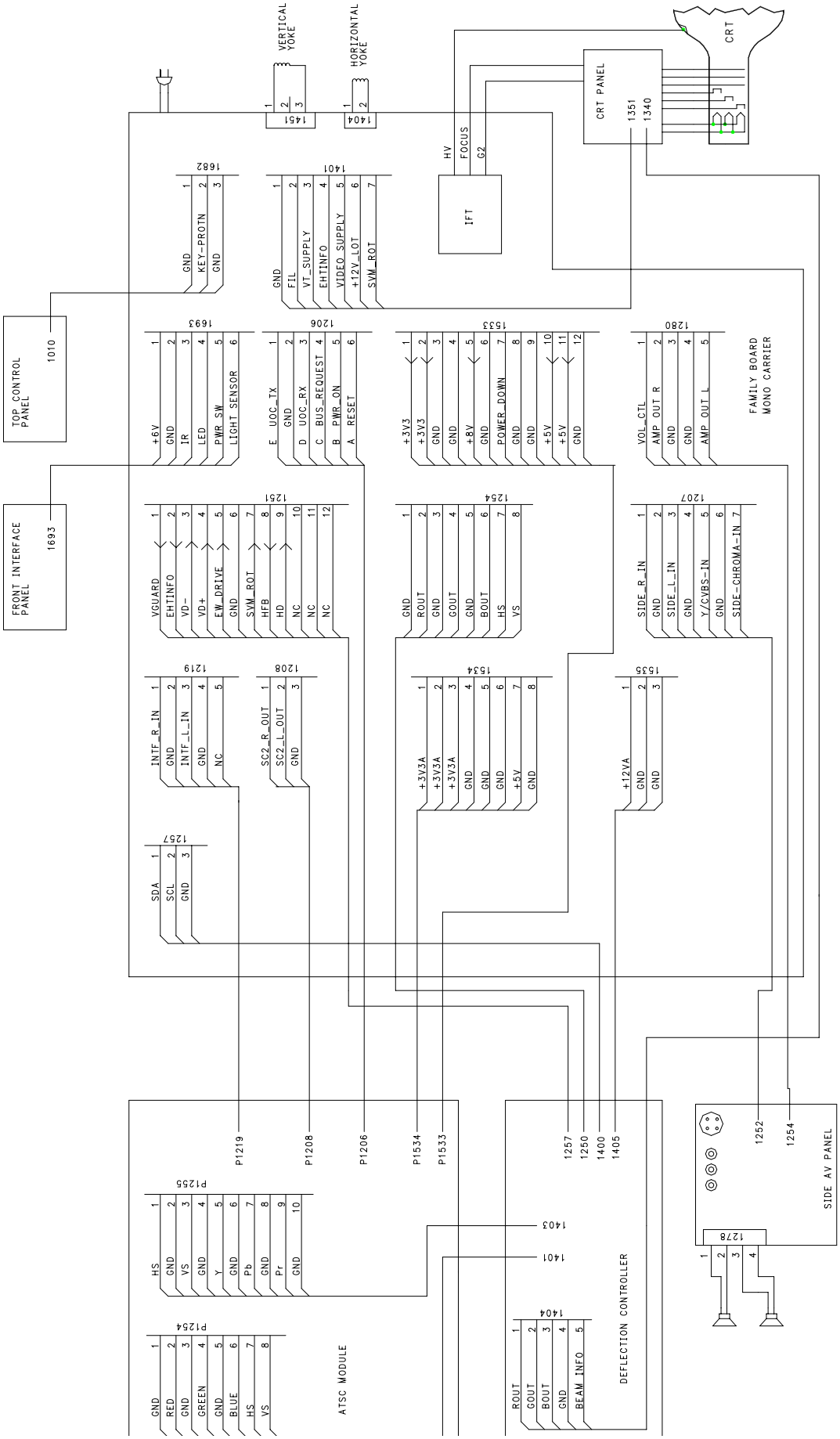

FIGURE 31 - WIRING INTERCONNECT DIAGRAM

System Control (Figure 32)

The Main system control is performed by the microprocessor located in the Hercules, IC 7200. The customer communicates with the processor via the IR sensor and Keyboard. The I2C bus communicates with the Tuner 1000 and the EEPROM 7601 located on the Family board. It also communicates with the TV Signal Processor 7402 and Deflection Processor 7404 located on the Deflection Controller board.

The Hercules Processor communicates with the ATSC module via the A through E control lines. Line E is the Data transmit line. Line D is the Data receive line from the ATSC module. Line C is the Bus Request line. Line B gives the ATSC module the command to turn On when the set is switched On. Line A sends a reset command to the ATSC module when the set is turned On.

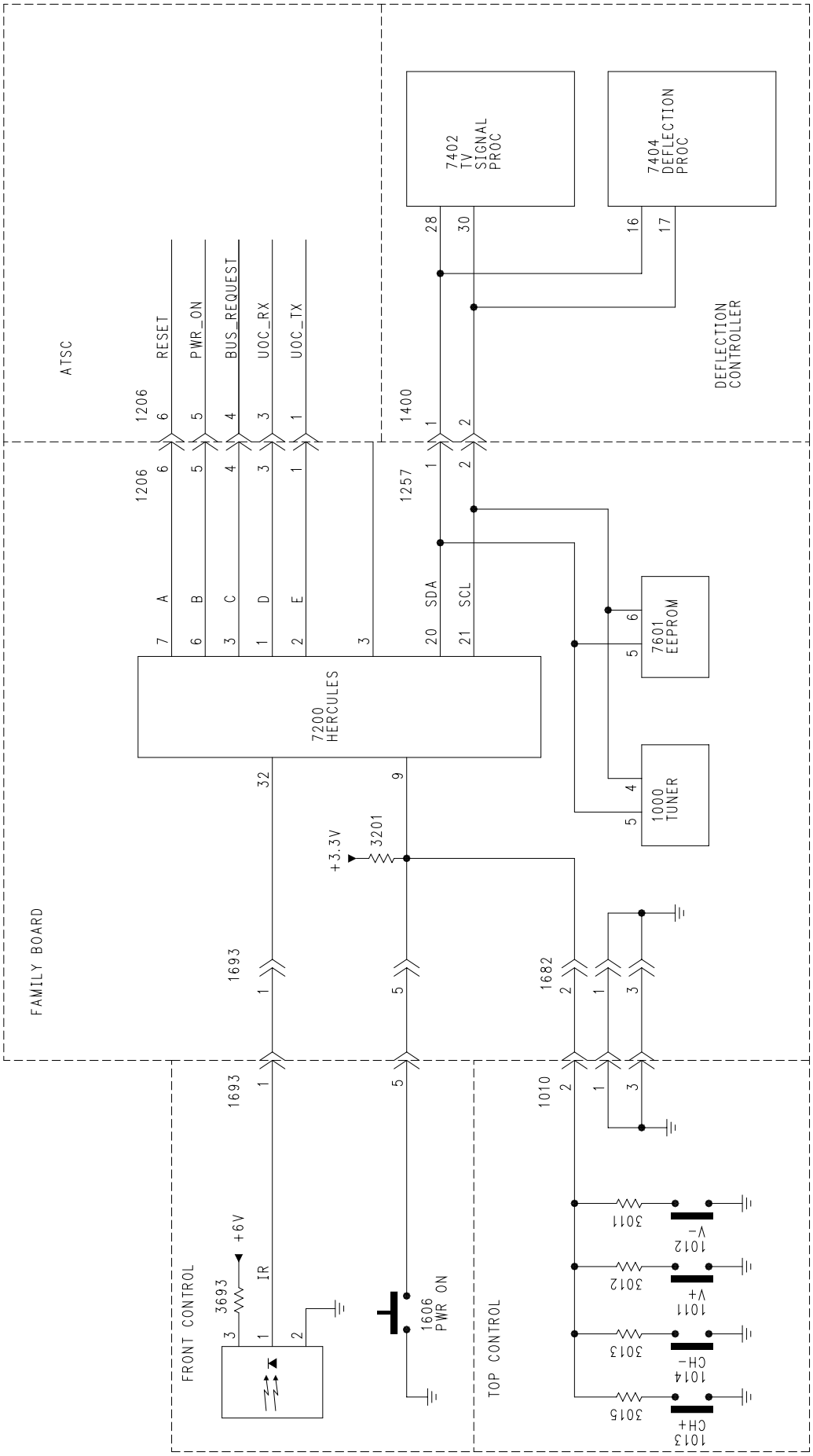

FIGURE 32 - SYSTEM CONTROL

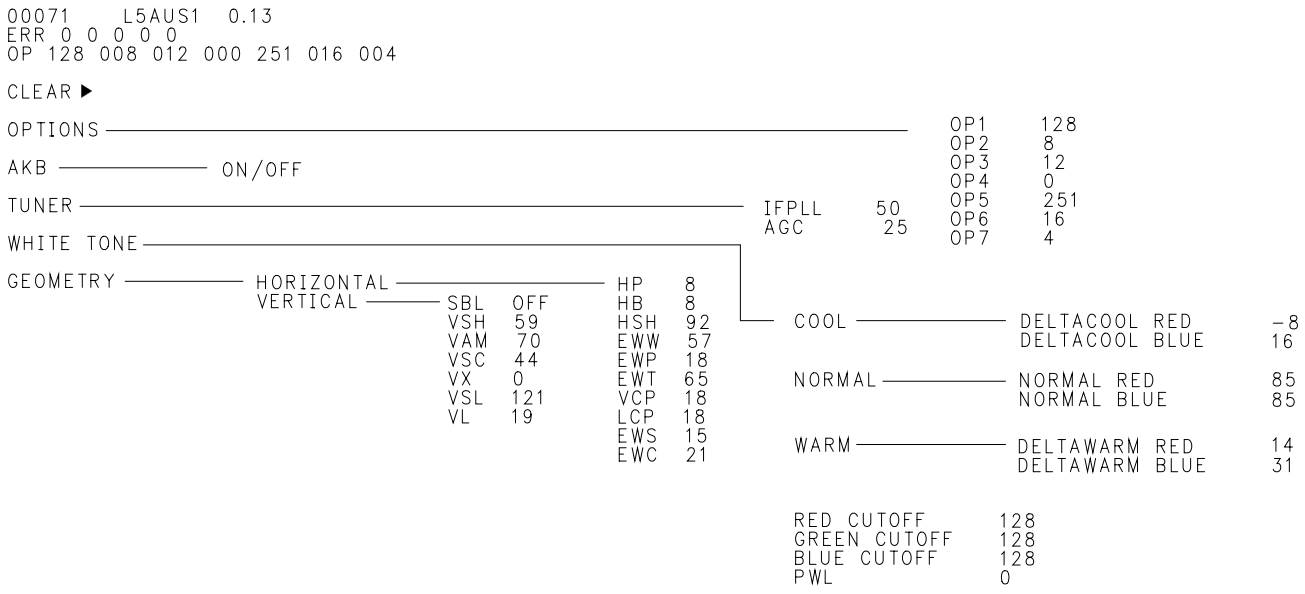

FIGURE 33 - SERVICE ALIGNMENT MODE

Service Alignment Mode SAM (Figure 33)

Making changes in the settings requires entering the SAM. To enter SAM, press 0 6 2 5 9 6 Info on the remote control. Use the cursor-up and cursor-down buttons to highlight a selection. Press the cursor-right, cursor-left buttons, or enter a value to make changes.

Customer Service mode CSM (Figure 34)

To enter the Customer Service Mode, press 1 2 3 6 5 4 on the remote control. This allows the customer to read settings after being directed to this mode by service personal. No changes can be made in this mode. The screen show is with the set in the Digital Mode. To

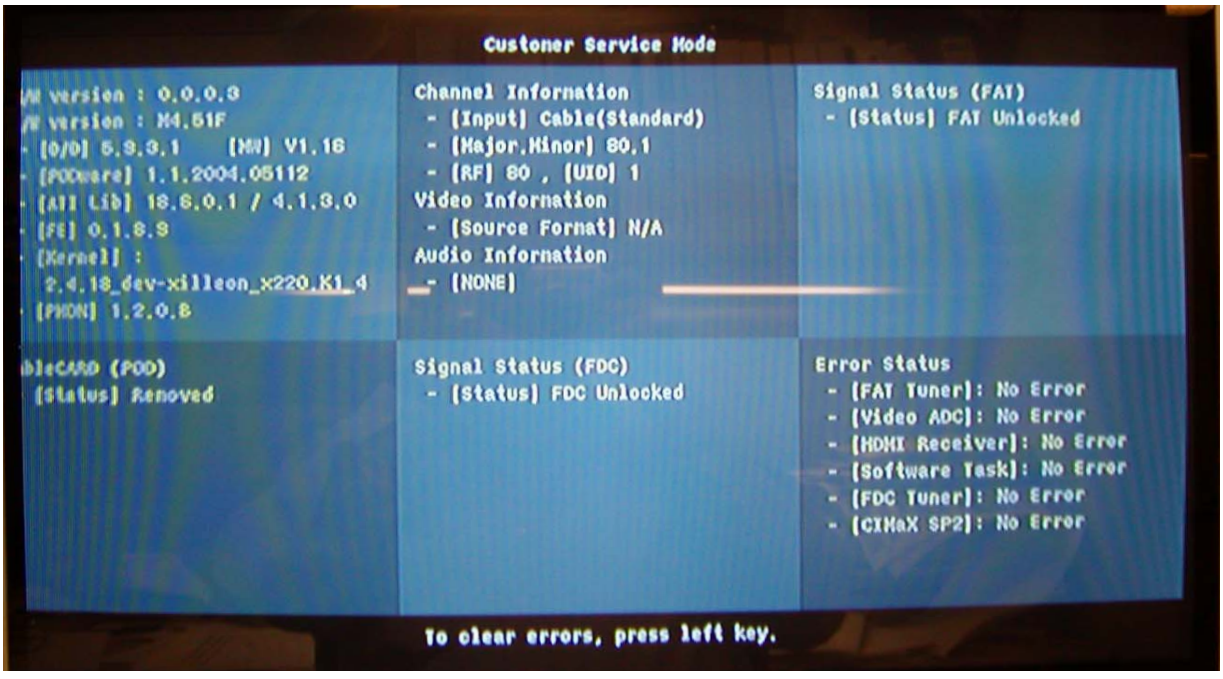

FIGURE 34 - CUSTOMER SERVICE MODE - DIGITAL

view the Analog settings, place the set in the Analog mode by pressing the D/A button on the remote and then re-entering the Customer Service Mode. (Figure 35) Refer to the Service manual for an explanation of the CSM and SAM settings.

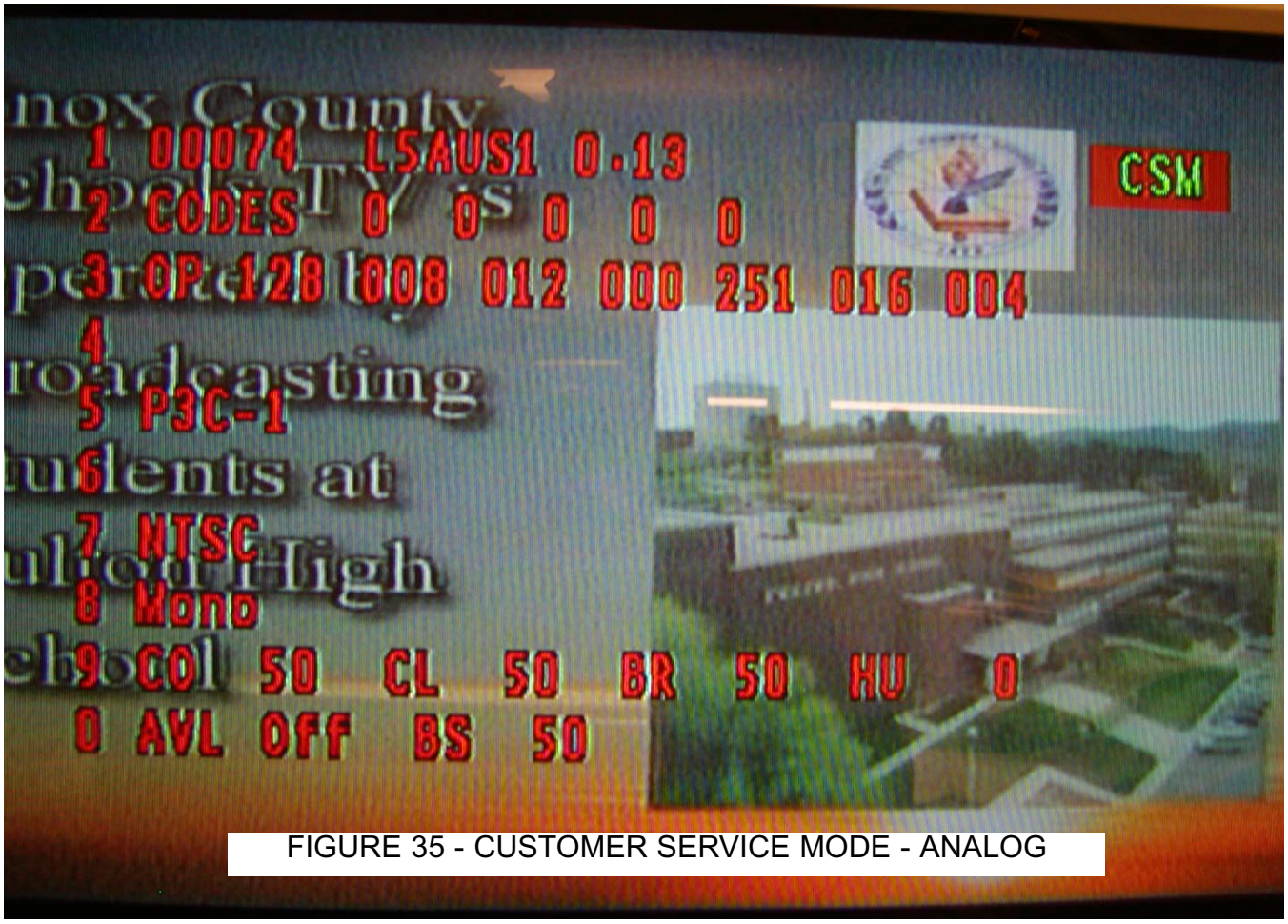

FIGURE 35 - CUSTOMER SERVICE MODE - ANALOG

SDM (Service Default Mode)

The Service Default Model allows the Error Codes, Operation Hours, and Software version to be read if the OSD is working. The SDM can be entered by pressing 0 6 2 5 9 6 Menu on the remote control.

If the picture is not present, error codes can be read by shorting the SDM Jumper to ground. Remove power from the set and short the SDM jumper, 9252, to ground. Reapply power and turn the set On. After a short period of time, the Power LED will blink to indicate the errors. The LED will blink the number of times for the first error. The LED will then pause and then blink the number of times for the second error, etc.

If a critical error exist, the Power LED will blink when the set is turned On for the number of times for the error.

Abbreviation list

Abbreviation	Description
1080i	1080 visible lines, interlaced
1080p	1080 visible lines, progressive scan
480i	480 visible lines, interlaced
480p	480 visible lines, progressive scan
ADC A/D	Analogue to Digital Converter
AFC	Automatic Frequency Control: control signal used to tune to the correct frequency
AGC	Automatic Gain Control: algorithm that controls the video input of the feature box
AM	Amplitude Modulation
AV	Audio Video
C-FRONT	Chrominance front input
CBA	Circuit Board Assembly (or PWB)
ComPair	Computer aided rePair
CSM	Customer Service Mode
CVBS	Composite Video Blanking and Synchronization
CVBS-EXT	CVBS signal from external source (VCR, VCD, etc.)
CVBS-INT	CVBS signal from Tuner
CVBS-MON	CVBS monitor signal
CVBS-TER-OUT	CVBS terrestrial out
DAC	Digital to Analogue Converter
DFU	Directions For Use: owner's manual
DNR	Dynamic Noise Reduction
DRAM	Dynamic RAM
DSP	Digital Signal Processing
DTS	Digital Theatre Sound
DVD	Digital Video Disc
EEPROM	Electrically Erasable and Programmable Read Only Memory
EPLD	Electronic Programmable Device
EXT	EXTernal (source), entering the set by cinches (jacks)
FBL	Fast Blanking: DC signal accompanying RGB signals
FLASH	FLASH memory
FM	Field Memory / Frequency Modulation
FMR	FM Radio
FRC	Frame Rate Converter
FRONT-C	Front input chrominance (SVHS)
FRONT-DETECT	Front input detection
FRONT-Y_CVBS	Front input luminance or CVBS (SVHS)
H	H_sync to the module
HD	High Definition
HDMI	High Definition Multimedia Interface
HP	HeadPhone
I2C	Integrated IC bus
I2S	Integrated IC Sound bus

IC	Integrated Circuit
IF	Intermediate Frequency
Interlaced	Scan mode where two fields are used to form one frame. Each field contains half the number of the total amount of lines. The fields are written in 'pairs', causing line flicker.
IR	Infra Red
IRQ	Interrupt ReQuest
Last Status	The settings last chosen by the customer and read and stored in RAM or in the NVM. They are called at start-up of the set to configure it according the customers wishes
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LINE-DRIVE	Line drive signal
LVDS	Low Voltage Differential Signalling, data transmission system for high speed and low EMI communication.
MPEG	Motion Pictures Experts Group
NVM	Non Volatile Memory: IC containing TV related data (for example, options)
OSD	On Screen Display
Progressive Scan	Scan mode where all scan lines are displayed in one frame at the same time, creating a double vertical resolution.
RAM	Random Access Memory
RC	Remote Control transmitter
RC5	Remote Control system 5, the signal from the remote control receiver
RGB	Red, Green, and Blue. The primary colour signals for TV. By mixing levels of R, G, and B, all colors (Y/C) are reproduced.
RGBHV	Red, Green, Blue, Horizontal sync, and Vertical sync
ROM	Read Only Memory
SAM	Service Alignment Mode
SIF	Sound Intermediate Frequency
SC	SandCastle: two-level pulse derived from sync signals
SCL	CLock Signal on I2C bus
SDA	DAta Signal on I2C bus
SDRAM	Synchronous DRAM
SIF	Sound Intermediate Frequency
STBY	STandBY
VGA	Video Graphics Array
XTAL	Quartz crystal
YPbPr	Component video (Y= Luminance, Pb/Pr= Colour difference signals)
Y/C	Luminance (Y) and Chrominance (C) signal
Y-OUT	Luminance-signal